Int. J. Electrochem. Sci., 10 (**2015**) 3291 - 3300

International Journal of
ELECTROCHEMICAL
SCIENCE
www.electrochemsci.org

$CdCl_2$ Treatment on Chemically Deposited CdS Active Layers in Thin Film Transistors

T. Mendívil-Reynoso[1,2], *L. P. Ramírez-Rodríguez*[3,*], *M.A. Quevedo-López*[4], *R. Ramírez-Bon*[5], *S.J. Castillo*[6]

[1]Centro de Investigación en Materiales Avanzados, Miguel de Cervantes 120, Complejo Industrial. CP 31109 Chihuahua, Chih., México.
[2]Departamento de Física, Universidad de Sonora, Apdo. Postal 1626, CP. 83000 Hermosillo, Sonora, México.
[3] Universidad Estatal de Sonora, Ley Federal de Trabajo Col. Apolo S/N CP 83100. , Hermosillo, Sonora, México.
[4] Department of Materials Science and Engineering, The University of Texas at Dallas, Richardson 75083, TX, USA
[5]Centro de Investigación y Estudios Avanzados del IPN. Unidad Querétaro, Apdo. Postal 1-798, C.P. 76001, Querétaro, Qro., México
[6]Departamento de Investigación en Física, Universidad de Sonora, Apdo. Postal 5-088, CP. 83000, Hermosillo, Sonora, México
[*]E-mail: tycho267@hotmail.com

Received: 12 December 2014 / *Accepted:* 22 January 2015 / *Published:* 24 February 2015

In this work CdS layers were deposited by an ammonia-free chemical bath deposition process on SiO_2/p-Si substrates as active layers of thin film transistors (TFT). The electrical characteristics of the CdS-based TFT with different channel lengths were analyzed after thermal annealing in forming gas combined with previous immersion in $CdCl_2$ saturated solution. The annealing temperatures were 100, 200 and 300 °C. To determine the effects of the $CdCl_2$ treatment on the device electrical parameters, devices with and without previous immersion in $CdCl_2$ were thermal annealed in forming gas and analyzed. The results show that the thermal annealing processes at 100 and 200 °C do not improve the electrical characteristics of the devices in both conditions. The annealing at 300 °C in both conditions improves noticeably the electrical performance of the devices attaining mobilities of the order of 5 cm^2/Vs, threshold voltage in the range -1.5-10 V, swing voltage in the range of 1.65-9 V and I_{on}/I_{off} current ratio of the order 10^3-10^6.

Keywords: $CdCl_2$ treatment; Chemical bath deposition; electrical properties; thin film transistors.

1. INTRODUCTION

CdS is an n-type II-VI semiconductor with a wide and direct energy band gap of 2.4 eV [1], which has been studied for decades because its important technological applications. More recently, the interest on CdS has increased considerably because the specific application as window layer in CdTe-CdS [2] and CIGS-CdS thin film solar cells [3-4]. Among the different deposition methods to elaborate CdS thin film are: chemical bath deposition (CBD) [5], radio frequency (r.f.) sputtering [6], spray pyrolysis [7], electrodeposition [1,8], among others. The CBD method stands out because its simplicity and low cost. Chemically deposited CdS thin films are homogeneous, stoichiometric, hard, well-adhered to substrate, etc. That is why CBD method is widely used to obtain CdS films for applications such as window layer in thin film solar cells and semiconductor active layer in thin film transistors [5]. When semiconductor films are used as active layers in semiconductor devices, it is very common the application of thermal treatments to improve their structural and electrical characteristics and therefore the performance of these devices. For example, the so-called $CdCl_2$ treatment is an additional step in the CdS-CdTe solar cell fabrication consisting in the exposure of the solar cell to a Cl-O ambient at high temperature, typically 400-500 °C [9]. This process improves considerably the efficiency of the solar cell by increasing the CdTe grain size and by promoting the interdiffusion at the CdS/CdTe interface [10]. Before the development of this process, this type of thin film solar cell attained efficiency less than 10% and nowadays the efficiency has increased up to about 20%, due mainly, among other reasons, to the improvement of the $CdCl_2$ treatment. Another conventional post-deposition process is forming gas annealing. Forming gas is a reducing gas which consists in the mixture of H_2 and N_2 with typical proportions 10 and 90 %, respectively. By using forming gas annealing it is possible to passivate defects, reduce oxidation and increase the crystallinity, conductivity and mobility of semiconductor layers. It has been shown that forming gas annealing increases the mobility and reduces the threshold voltage in thin film transistors; in the case of solar cells, this treatment can improve the fill factor to increase the solar cell efficiency [11].

The $CdCl_2$ treatment has been studied mainly on the CdTe layers because the modifications of this absorbent layer have stronger impact on the solar cell performance. Nevertheless, the effects of $CdCl_2$ treatments on CdS thin films have been also reported in a number of papers. In the work by Wan [12], it was studied the recrystallization process in CdS films with and without $CdCl_2$ coating layer. It was found that CdO and $CdSO_4$ oxides were formed in the films without the $CdCl_2$ layer; and that the thin $CdCl_2$ layer prevented the oxidation of the CdS films. $CdCl_2$ treatment also improves the crystalline quality of CdS films [9-13]. Forming gas annealing on CdS thin films has also been studied. In a recent paper [14], the structural and optical properties of CdS thin films, deposited by a hot plate method, were improved by forming gas annealing at 400 °C. In previous papers, we have found that forming gas annealing at 250 °C of CdS and PbS active layers enhances considerably the electrical behavior of thin film transistors [15,16]. The improved crystallinity of the annealed CdS and PbS active layers results in the increased mobility of the devices.

A field effect transistor (FET) can be elaborated as a thin film transistor (TFT); its operation principles are similar to those of the metal oxide semiconductor field effect transistor (MOSFET). Common-gated TFTs are relatively easy to fabricate by first depositing the semiconductor active layer

on a Si/SiO_2 substrate to get the semiconductor-dielectric system of the device. Then, two parallel metallic pads are deposited on the semiconductor layer as source/drain contacts, followed by a metal contact on the back of the doped silicon wafer, which acts as the gate of the transistor. By analyzing the electrical response of these devices, important conclusions can be attained regarding the physical characteristics of the semiconductor and dielectric layers. Therefore, the employment of this device methodology can be used to optimize the characteristics of semiconductor and dielectric layers as a function of deposition and post-deposition parameters. Furthermore, TFT devices have been intensively studied for potential applications in chemical and photodetecting devices, biosensors and flat panel displays [17,18,19,20]. In fact, another important application of CdS films has been as active layer in TFT devices. CdS active layers have shown good performance with channel mobility comparable to those of amorphous silicon ones, which are the semiconductor layers currently employed in active matrix liquid crystal displays. For this application, the characteristics of CdS active layers obtained by the CBD method are quite appropriated and a number of papers have been published about the performance of chemically deposited CdS as active layers in TFT devices [21,22,23]. In our group, we have developed an ammonia-free CBD method, based on sodium citrate as the complexing agent, to obtain CdS thin films with excellent crystalline and optical characteristics [24,25,26]. These ammonia-free CBD-CdS layers have shown very good performance as window layers in CdS-CdTe solar cells and in active layers in TFT devices [15,27]. These CdS layers attained channel mobilities of the order of 10^{-1} and 25 $cm^2V^{-1}s^{-1}$ in TFT devices using SiO_2 and HfO_2 layers as the gate dielectric, respectively [15,28]. For the case of the devices with SiO_2 dielectric layer it was found that forming gas annealing improved considerably the electrical response of the devices.

In this work we report further characterization on forming gas annealed CdS films obtained by an ammonia-free CBD method and their performance as active layers in TFT devices, using thermal SiO_2 as dielectric gate. The forming gas treatments were performed at temperatures between 100 and 300 °C on as grown CdS layers and on CdS layers which were previously immersed in a saturated $CdCl_2$ solution. We report in this paper the influence of both types of forming gas treatments on the electrical behavior of TFT devices fabricated with these CdS layers.

2. EXPERIMENTAL DETAILS

The TFT devices were fabricated on RCA cleaned p-Si wafers with 100 nm thermal SiO_2 layer as the dielectric gate of the device. The chemical deposition of the CdS layers on the SiO_2/p-Si substrates was done in a reactive solution prepared in a 100 ml beaker by the sequential addition of 15 ml of 0.05 M cadmium chloride ($CdCl_2$,Baker, 99.3%), 15 ml of 0.5 M sodium citrate ($C_6H_5O_7Na_3$, Baker, 99.1%), 5 ml of 0.5 M potassium hydroxide (KOH, Baker, 89.13%), 5 ml of pH 10 buffer solution (Baker) and 7.5 ml of 0.5 M thiourea ($CS(NH_2)_2$, Baker, 99.6%). The solution was diluted with deionized water to complete a total volume of 100 ml. The beaker with the reaction solution was immersed in a water bath at 70 °C. For the deposition of source and drain contacts, a photoresist layer was deposited on the CdS layer, UV exposed through a shadow mask and developed. The shadow mask consists of pairs of rectangular patterns that represent sets of parallel electrodes (source and

drain) whose separations (channel length) were L=80, 40 and 20 μm and the channel width, W=450 μm. A 100 nm gold layer was deposited on each sample by e-beam evaporation. The gold source/drain contacts were formed using lift-off process. Chromium (10 nm) and gold (100 nm) were evaporated on the back side of the p-Si wafer to form the back side contact (gate). Two kinds of treatments were used to build the TFT devices; the samples with three different lengths channel were thermal annealed at different temperatures 100, 200 and 300 ^{o}C in forming gas (90% N_2 +10% H_2) during one hour. On the other hand, another 3 samples were immersed in a saturated solution of $CdCl_2$, then every sample were thermal annealed at 100, 200 and 300 ^{o}C during one hour in forming gas. The electrical response of all the CdS-based TFT devices was determined measuring current versus voltage curves at room temperature in a probe station using a 4200 Keithley semiconductor parameter analyzer.

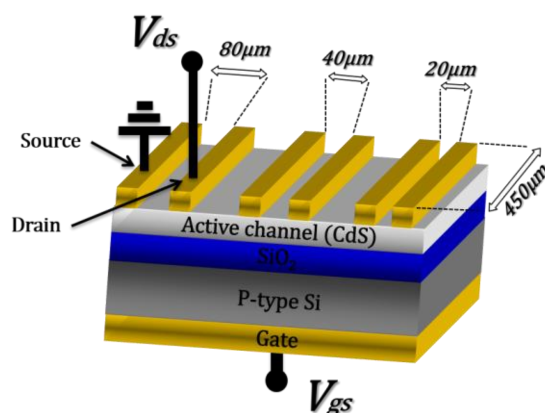

Figure 1. Schematic cross-section of the bottom-common gate CdS based TFT configuration.

3. RESULTS AND DISCUSSION

The electrical behavior of the as grown and annealed CdS-based TFT devices was analyzed from drain current versus drain voltage (I_{ds} vs V_{ds}) and drain current versus gate voltage (I_{ds} vs V_{gs}) measurements. The I_{ds} vs V_{ds} family of curves were measured at different V_{gs} values to confirm the proper behavior of the electrical output of the devices, meanwhile I_{ds} vs V_{gs} curves were measured at a V_{ds} values in the saturation region to determine the electrical parameters of the devices, namely channel mobility, threshold voltage and swing voltage.

As reported in previous papers, the thermal annealing in forming gas improves considerably the performance of CdS-based TFT devices, therefore we present the results for the devices annealed at 300 °C in forming gas with and without previous immersion in $CdCl_2$ solution. The results for all CdS-based TFT analyzed devices are summarized in table 1, shown below. Figure 2 shows the electrical characteristics of the TFT devices with CdS layer annealed in forming gas at 300 °C; a) and b) graphs correspond to a device with 40μm channel length and c) and d) to a device with 80 μm channel length. The family curves of both devices, Figs. 2 a) and 2 c), measured at V_g values between 0 and 40 V, shows the typical linear behavior at low voltages and current saturation al higher voltages.

The first transistor attains the saturation current at lower voltage than the second one for each gate voltage. In both cases the order of magnitude of the maximum saturation current was around 1 mA, being the saturation currents slightly larger in the first transistor than in the second one. The dotted parabolic curve in these graphs crosses the family curves at about the starting points of the saturation currents.

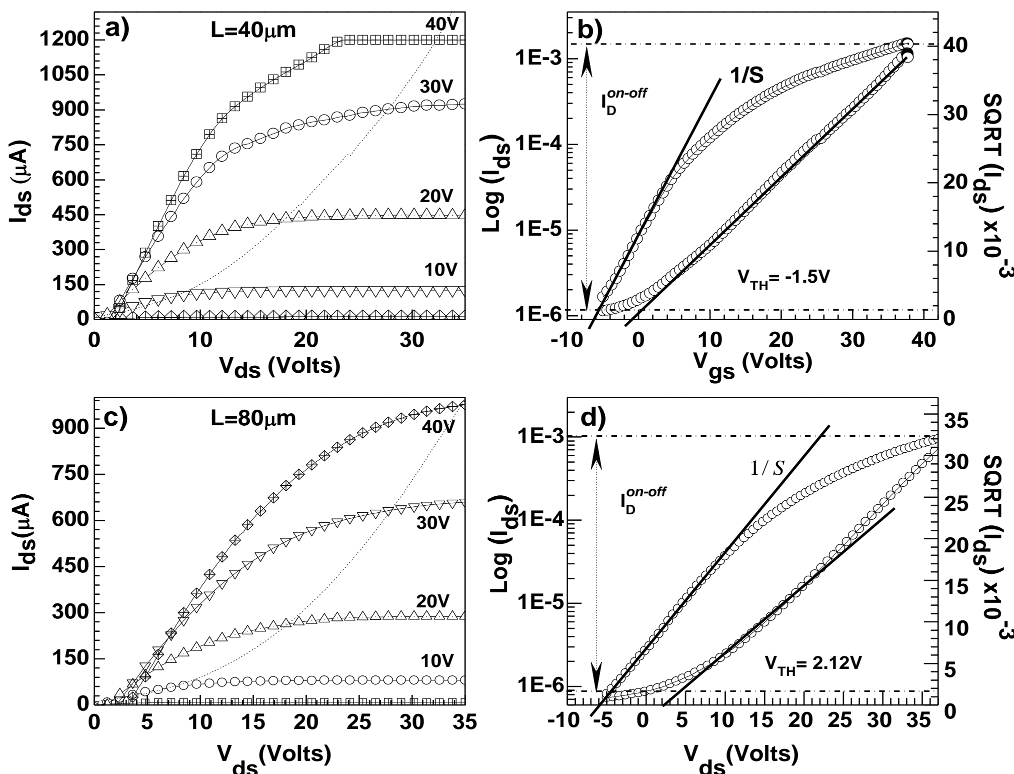

Figure 2. Electrical behavior of the TFT devices with CdS channel layer annealed in reductive forming gas atmosphere at 300°C. a) Family of I_{ds} versus V_{ds} curves of the TFT device with 40 μm channel length, b) Plots of log I_{ds} versus V_{gs} (left axis) and $(I_{ds})^{1/2}$ versus V_{gs} (right axis), measured at V_{ds} =40 V for the device with 40 μm channel length. The corresponding graphs for the device with 80 μm channel length are shown in c) and d), respectively.

The graphs in Fig. 2b) and 2 d) display the transfer characteristics of both transistors, the left axis corresponds to I_{ds} in log scale and the right axis to the square root of I_{ds}, both quantities as a function of V_{gs}. From the I_{ds}-V_{gs} curves it was obtained the I_{on}/I_{off} current ratio, which is of the same order in both devices, about 10^3 and the swing voltage, S, which values were 6.65 and 6.07 V/decade for the first and second transistor, respectively. On the other hand, from the linear fit to the $\sqrt{I_{ds}}$ -V_{gs} curves, shown as solid lines, it were determined the values of the channel mobility, μ_{sat}, and threshold voltage, V_{th}, of the devices. The channel mobility for the 40 μm channel length transistor is 5.15 cm^2/Vs and for the 80 μm channel length device is 8.3 cm^2/Vs, as expected, the channel mobility is proportional to the channel length. The threshold voltages for these transistors are -1.5 and 2.12 V, respectively. The negative (positive) value of V_{th} of the first (second) transistor indicates that this

device operates in the depletion (enhancement) mode, that is, at V_{gs}=0 V, the device is in the on-state (off-state).

In Fig. 3 there are shown the graphs which depict the electrical behavior of the TFT devices with CdS layer immersed in the $CdCl_2$ solution and subsequently annealed in forming gas at 300 °C. In this case, three devices were analyzed with 20, 40 and 80 μm channel length, respectively. The family curves of the three devices, Figs. 3 a), 3 c) and 3 e), show a good saturation current behavior at high voltage, with maximum saturation current increasing with decreasing channel length. The saturation current values between 0.4-0.9 mA are lower for these devices compared to those in Fig. 2. Notice that also in this case the quadratic behavior of the starting points of the saturation currents is valid (dotted parabolic curves), for gates voltages values above the threshold voltage. The transfer characteristics of these devices, Figs. 3 b), 3 d) and 3 f) display lower current in the off-state, I_{off}, of the order of 10^{-9}. Since the observed current in the on-state, I_{on}, is of the same order of 10^{-3} as in the other devices (Fig. 2), the I_{on}/I_{off} current ratio increases to 10^6 for these devices. The swing voltage also improves in these devices, which values were 1.7, 1.67 and 1.65 V/decade for the transistors with 20, 40 and 80 μm channel length, respectively. The threshold voltage and channel mobility, obtained from the linear fit to the $\sqrt{I_{ds}}$ versus V_{gs} curves, were 8.63 V and 2.73 cm^2/Vs, 9.86 V and 4.32 cm^2/Vs, and 0.18 V and 5.49 cm^2/Vs, for the transistors with 20, 40 and 80 μm channel length, respectively.

The results obtained for all the measured devices are summarized in Table 1. According to the values of the electrical parameters in this table, the annealing processes at 100 and 200 °C of the CdS layer in both conditions, forming gas with and without $CdCl_2$ immersion, do not improve the electrical response of the devices with channel mobility of the order of 10^{-2}-10^{-3} cm^2/Vs, threshold voltage between 8-20 V and I_{on}/I_{off} current ratio between 10^2 and 10^3. The best results with strong modifications in the electrical performance of the CdS-based TFT devices were obtained by annealing the CdS layers at 300 °C in both conditions.

All the measured performance parameters of the CdS-based transistor were improved by annealing at this temperature. The annealing in forming gas at 300 °C without the $CdCl_2$ immersion produced the devices with highest mobility and lowest threshold voltage; however, the I_{on}/I_{off} current ratio and swing voltage were not improved as compared with the devices annealed at 200 °C. On the other hand, the devices with CdS layer immersed in $CdCl_2$ solution and annealed at 300 °C in forming gas had the highest the I_{on}/I_{off} current ratio of the order of 10^6 and the lowest swing voltage in the range 1.65-17 V/decade. The channel mobility of these devices was in the range 2.73-5.49 cm^2/Vs, values which are in the order of those of the devices annealed at 300 °C without immersion in $CdCl_2$. The parameter of these devices which was not improved with annealing temperature was threshold voltage which values were in the range 8.63-10.18 V/decade. However, although this drawback, the immersion in $CdCl_2$ solution and subsequent annealing process in forming gas at 300 °C improves strongly the I_{on}/I_{off} current ratio, increasing it in three orders of magnitude, and the swing voltage decreasing it to about a quarter the value measured in the devices without the immersion in $CdCl_2$ solution.

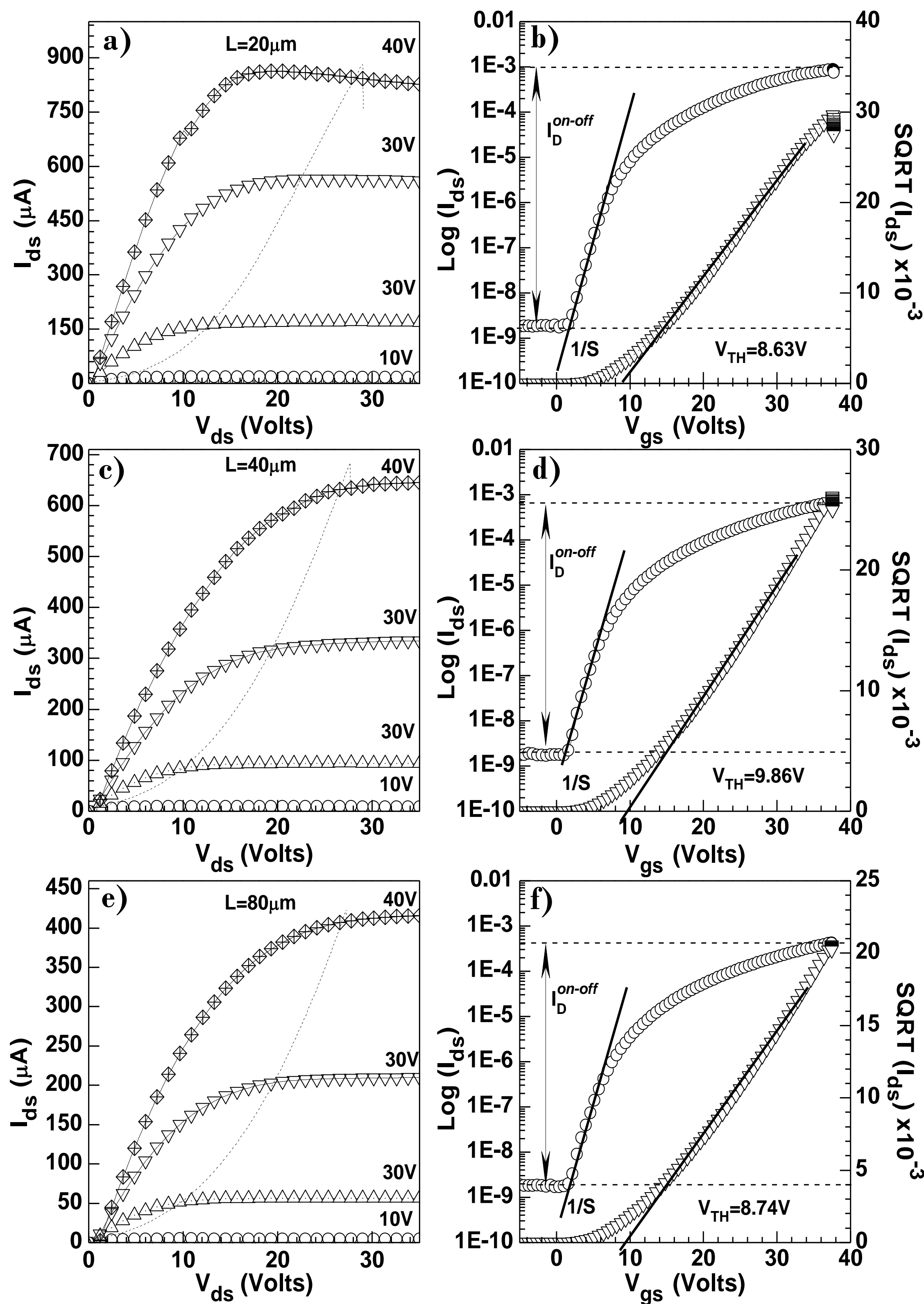

Figure 3. Electrical behavior of the TFT devices with CdS channel layer immersed in a $CdCl_2$ solution and then annealed in reductive forming gas atmosphere at 300°C. a) Family of I_{ds} versus V_{ds} curves of the TFT device with 20 μm channel length, b) Plots of log I_{ds} versus V_{gs} (left axis) and $(I_{ds})^{1/2}$ versus V_{gs} (right axis), measured at V_{ds} =40 V for the device with 20 μm channel length. The corresponding graphs for the devices with 40 and 80 μm channel length are shown in c), d), e) and f), respectively.

Table 1. Electrical parameters of the TFT devices with CdS channel layer annealed in reductive forming gas atmosphere at 100, 200 and 300°C, without (H_2+N_2) and with $CdCl_2$ ($CdCl_2$-N_2+H_2) previous immersion in $CdCl_2$ solution.

$N_2 + H_2$	μ (cm^2/Vs)	V_{th} (volts)	I_{on-off}	S	$CdCl_2$-$N_2 + H_2$	μ (cm^2/Vs)	V_{th} (volts)	I_{on-off}	S
100°C L=80μm	-	-	-	-	100°C L=80μm	0.0004	23	~10^2	7.48
L=40μm	0.0046	20.1	~10^2	8.17	L=40μm	0.0064	5	~10^3	4.29
L=20μm	0.0029	12.45	~10^2	7.33	L=20μm	0.003	11.23	~10^3	
200°C L=80μm	0.4	7.32	~10^3	3	200°C L=80μm	0.036	9.99	~10^3	3.181
L=40μm	0.084	7.8	~10^3	2.8	L=40μm	0.0158	7.4	~10^3	3.13
L=20μm	0.045	14.7	~10^3	3.5	L=20μm	0.01	9.54	~10^3	4.1
300°C L=80μm	8.3	2.12	~10^3	6.08	300°C L=80μm	5.49	10.18	~10^6	1.65
L=40μm	5.15	-1.5	~10^3	6.55	L=40μm	4.32	9.86	~10^6	1.672
L=20μm	5.26	0.573	~10^3	9	L=20μm	2.73	8.63	~10^6	1.7

The thermal annealing at high temperature of polycrystalline semiconductors in several reactive atmospheres improves the crystalline quality by increasing the grain size and compacting the grains in tighter microstructures, reduces and passives defects including those at the grain boundaries, which play an important role in the electrical transport properties of these materials. The dispersion and trapping of charge carriers at the grain boundaries of polycrystalline semiconductors reduce the carrier mobility and then the electrical resistivity. That is why the electron mobility reported for CdS polycrystalline films is much lower than the corresponding value of bulk crystalline CdS, which is 210 $cm^2V^{-1}s^{-1}$ [29]. Therefore, we can assign the low channel mobility of the devices with CdS layer annealed at 100 and 200 °C to the polycrystalline character of the CdS films. As mentioned above, annealing is a standard step in the fabrication of CdS-based TFT devices in order to improve the electrical characteristics of the active layer and then the performance of the devices. For example, it has been reported that by annealing in vacuum at temperature of 300 °C, CdS-based transistors attained channel mobility of 0.5 $cm^2V^{-1}s^{-1}$, threshold voltage of 14 V and $I_{on}/I_{off} = 10^7$ [30]. In other case, by rapid thermal annealing at 500 °C, the CdS-based transistors had channel mobility of 1.5 $cm^2V^{-1}s^{-1}$, threshold voltage of 14 V and $I_{on}/I_{off} = 10^7$ [31]. By comparing with these and other results in literature about CdS-based transistors we found that the annealing at 300 °C in forming gas with and without immersion in $CdCl_2$ solution produces devices with performance parameters in the order or better than those reported in literature. Particularly it is noticeable the low threshold voltage of a few volts measured in the annealed devices without the immersion in $CdCl_2$ solution. However, taking into account all the performance parameters the annealing in forming gas after immersion in $CdCl_2$ solution produced the best devices, with very good values of I_{on}/I_{off} current ratio and swing voltage.

4. CONCLUSIONS

In this work we have reported that there exist some critical parameters or growing conditions that optimize the electrical output characteristics of CdS-based TFT devices. This study proved that annealing the CdS layer in reductive atmosphere of forming gas at 300°C, improved notably the drain current, threshold voltage and field effect mobility. In one device it was even attained the conversion of n-type enhancement mode transistor to n-type depletion mode. When the annealing in forming gas process is combined with previous immersion in $CdCl_2$ solution, this avoid the conversion of enhancement mode to depletion one and increased the I_{on}/I_{off} current ratio to 10^6 and reduced the swing voltage to values in the range 1.65-1.7 V.

ACKNOWLEDGEMENTS
The technical assistance of M. A. Hernández Landaverde, J.E. Urbina Alvárez, A. Jiménez Nieto and Carlos Alberto Avila Herrera is acknowledged. This work was supported by Conacyt-México.

References

1. M. Fathy, A.E.H.B. Kashyout, S. Elyamny, G.D. Roston and A.A. Bishara *Int. J. Electrochem. Sci*. 9 (2014) 6155.
2. K. Durose, P.R.Edwards, and D.P.Halliday. *J. Cryst. Growth* 197 (1999) 733.
3. N. Romeo, A. Bosio, R. Tedeschi, A. Romeo, and V. Canevari. *Sol Energ Mat Sol* C. 58 (1999) 209.
4. H. Komaki, A.Yamada, K. Sakurai, S. Ishizuka, Y. Kamikawa-Shimizu, K. Matsubara, S. Shibata and S. Niki. *Phys. Status Solidi* (a) 206 (2009) 1072
5. T. Mendivil-Reynoso, D. Berman-Mendoza, L.A. González, S.J. Castillo, A. Apolinar-Iribe, B. Gnade, M.A. Quevedo-Lopez and R. Ramírez-Bon. *Semicond. Sci. Tech* 26 (2011) 115010.
6. B.S. Moon, J.H. Lee, and H. Jung. *Thin Solid Films* 511 (2006) 299.
7. Y.Y. Ma and R.H. Bube. *J. Electrochem. Soc*. 124 (1977) 1430.
8. J. Nishino, S. Chatani, Y. Uotani, and Y. Nosaka. *J. Electroanal. Chem*. 473 (1999) 217.
9. Z.C. Feng, C.C. Wei, A.T.S. Wee, A. Rohatgi, and W. Lu. *Thin Solid Films* 518 (2010) 7199.
10. P.D. Paulson and V. Dutta. *Thin Solid Films* 370 (2000) 299.
11. Y.T. Cheng, J.J. Ho, W. Lee, S.Y. Tsai, L.Y. Chen, J.J. Liou, S.H. Chang, S. Shen and K.L. Wang. *Int. J. Photoenergy* 2010 (2010) 1.
12. L. Wan, Z. Bai, Z. Hou, D. Wang, H. Sun and L. Xiong. Thin Solid Films 518 (2010) 6858.
13. J. H. Lee and D. J. Lee. *Thin Solid Films* 515 (2007) 6055.
14. S.H. Mousavi, M.H. Jilavi, T.S. Müller, and P.W. de Oliveira. *J. Mater. Sci.-Mater. Electron*. 25 (2014) 2786.
15. G. Arreola-Jardón, L.A. González, L.A. García-Cerda, B. Gnade, M.A. Quevedo-López and R. Ramírez-Bon. *Thin Solid Films* 519 (2010) 517.
16. I.E. Morales-Fernández, M.I. Medina-Montes, L.A. González, L.A. García-Cerda, B. Gnade, M.A. Quevedo-López and R. Ramírez-Bon. *Thin Solid Films* 519 (2010) 512.
17. E. Bandiello, M. Sessolo, and H.J. Bolink. *J. Mater. Chem. C*. 2 (2014), 10277.
18. L. Maiolo, S. Mirabella, F. Maita, A. Alberti, A. Minotti, V. Strano, A. Pecora, Y. Shacham-Diamand and G. Fortunato. *Appl. Phys. Lett.* 105 (2014) 093501.
19. A. Nathan, S. Lee, S. Jeon and J. Robertson. *J. Display Technol*.10 (2013) 917.

20. W.Y. Chou, Y.S. Lin, L.L. Kuo, S.J. Liu, H.L. Cheng, and F.C. Tang. (2014). *J. Mater. Chem. C*. 2 (2014) 626.
21. F.Y. Gan and I. Shih. *IEEE Trans. Electron Devices* 49 (2002) 15.
22. C. Voss, S. Subramanian and C.H. Chang. *J. Appl. Phys*. 96 (2004) 5819.
23. B. Mereu, G. Sarau, E. Pentia, V. Draghici, M. Lisca, T. Botila and L. Pintilie. *Mater. Sci. Eng* B. 109 (2004) 260.
24. M.B. Ortuño-López, J.J. Valenzuela-Jáuregui, M. Sotelo-Lerma, A. Mendoza-Galván, R. Ramírez-Bon. *Thin Solid Films* 429 (2003) 34.
25. M.B. Ortuño-López, M. Sotelo-Lerma, A. Mendoza-Galván, R. Ramírez-Bon. *Thin Solid Films* 457 (2004) 278.
26. M.G. Sandoval-Paz, M. Sotelo-Lerma, A. Mendoza-Galván, R. Ramírez-Bon. *Thin Solid Films* 515 (2007) 3356.
27. R. Ochoa-Landín, J. Sastre-Hernández, O. Vigil-Galan and R. Ramírez-Bon. *Sol. Energy* 84 (2010) 208.
28. A.L. Salas-Villaseñor, I. Mejía, J. Hovarth, H.N. Alshareef, D.K. Cha, R. Ramírez Bon, B.E. Gnade and M.A. Quevedo-López. *Electrochem. Solid State Lett*. 13 (2010) H313–H316.
29. J. I. Pankove, Optical Processes in Semiconductors, (Dover Publications Inc., New York, 1971).
30. J.H. Lee, J.W. Yoon, I.G. Kim, J.S. Oh, H.J. Nam and D.Y. Jung. *Thin Solid Films* 516 (2008) 6492.
31. Y.-J. Chang, C.L. Munsee, G.S. Herman, J.F. Wager, P. Mugdur, D.-H. Lee and C.-H. Chang. *Surf. Interface Anal*. 37 (2005) 398.

© 2015 The Authors. Published by ESG (www.electrochemsci.org). This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution license (http://creativecommons.org/licenses/by/4.0/).