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Short Communication

Effects of Doped Stannum in the Fabrication of Zinc-Oxide Thin-Film Transistors

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A sol-gel method was applied with acetates as precursors under standard atmospheric conditions to fabricate ZnO semiconducting thin-films. We evaluated the performances of thin-film transistor (TFT) which has a ZnO active channel layer and the effects of stannum (Sn) doping on the threshold voltage of ZnO TFTs at a low temperature (300 ℃), which was compared with the performances of the un-doped ZnO and stannum-doped zinc oxide (ZTO) TFT. The electrical characteristics of thin-films and TFTs doped with stannum concentrations of 0.3 mole ratio were examined; and reductions at the threshold voltage of 5.6 V were found. At 300 ℃, it was observed that the stannum-doped zinc oxide (ZTO) device has a mobility of 4.2×10^{-4} cm^2/V-s, a threshold voltage of 5.3 V, and an on/off current ratio of 10^4.

Keywords: Thin-film transistor, threshold voltage, zinc tin oxide, ZnO, ZTO

1. INTRODUCTION

Generally, electrodes in displays [1] have used metal oxide thin-films, such as In_2O_3, SnO_2, and ZnO. Recently, in drive transistors [2, 3], an active channel layer has been intensively studied for application. These continuous processes typically involve high vacuum deposition, such as chemical vapor deposition (CVD) and physical vapor deposition (PVD), which contribute to high costs. The solution processes used for ZnO film deposition in atmospheric environments include the sol-gel method and chemical bath deposition (CBD) [4, 5]. By using a sol-gel method, ZnO TFTs fabricated can be achieved using halide and organic precursors in numerous solvents [6-10]. Chlorides are used

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as precursors for sol-gel ZnO materials; however, chloride is toxic. In this study, the sol-gel processed ZnO TFT was derived from acetate salts [11]. Numerous studies have demonstrated transparent ZnO TFTs doped with combinations of Ga, In, and Sn, such as indium zinc oxide (IZO) [11], indium gallium zinc oxide (GIZO) [12], and zinc tin oxide (ZTO) [13]; however the cost of indium is high. The ionic radius of Sn^{4+} is 0.69 Å and smaller compared with the ionic radius (0.74 Å) of Zn^{2+}; thus, Sn^{4+} ions can replace Zn^{2+} ions in substitutional sites [14]. However, few studies have examined Sn doped ZnO TFTs made by using a sol-gel process [15, 16].

This ZnO semiconductor thin-films made using a sol-gel method are examined at various annealing temperatures under standard atmospheric conditions, and acetates are used as precursors [17-24]. The performance of TFTs with a ZnO active channel layer and the compatibility of Sn doped ZnO (ZTO) TFT for various doping levels with a low temperature process (300 ℃) were evaluated [25-31].

2. EXPERIMENTAL DETAILS

The ZnO and ZTO precursor solutions synthesized uses zinc acetate dihydrate and tin (IV) acetate. The solutions (0.05M in metal precursors) were made in 2-methoxyethanol (2ME). The Sn/Zn molar ratio of ZTO precursor solutions was 0.3 mole ratio. The metal oxide solutions were stirred at 80 ℃ for 30 min before applying spin-coating, as shown in the solution flow chart in Fig. 1 [15, 31].

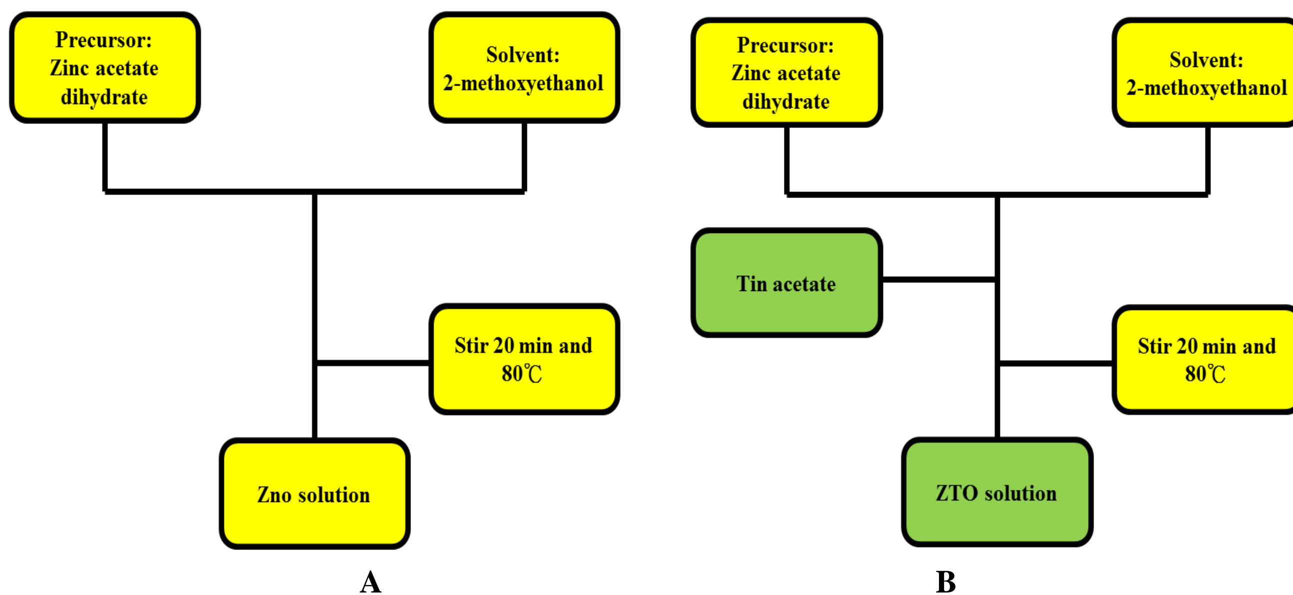

Figure 1. The preparation of the (a) ZnO, (b) ZTO solution use the sol-gel method

RCA clean was used to treat all prepared p-type silicon wafers, and then a SiO_2 film with a thickness of approximately 100 nm was grown by thermal oxidation. After SiO_2 formation, oxygen plasma was used to treat the surface for 30 s. ZnO or ZTO films deposited was made by spin coating at

1000 rpm for 30 s under an ambient temperature of 25 °C. ZnO or ZTO solution was spin to obtain the film that was then annealed for 1 hour at 300 °C in air. Finally, a thermal evaporation (pressure 10^{-6} Torr) process was used to back plate the wafer with Al, and 300 nm Al was defined as the gate electrode followed by a shadow mask to define the source and drain, which were both plated with Al = 300 nm. Fig. 2 shows a schematic cross-sectional view of the ZnO and ZTO structure. The devices were measured using an Agilent 4156.

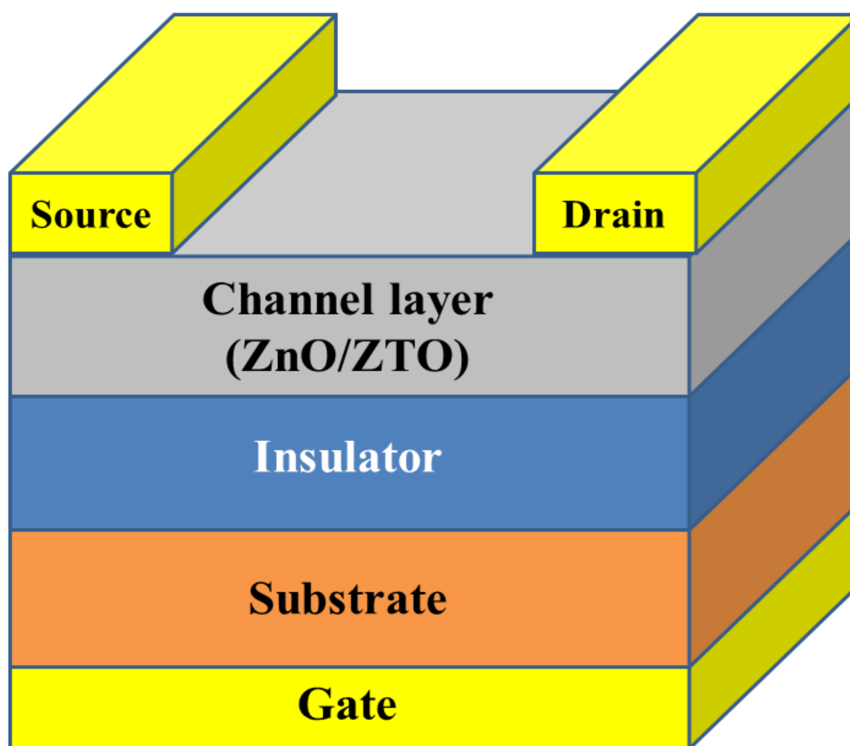

Figure 2. A schematic cross-sectional view of the ZnO and ZTO Thin-Film Transistors structure.

3. RESULTS AND DISCUSSION

The surface morphology of the thin-film is crucial in a transistor. Images were acquired in contact mode, and the collected scan area was 1 μm×1 μm. Fig. 3 shows the AFM images of the sol-gel-derived ZnO thin films. After exposure for 1 hour at 300 ℃ in air, the sample had a root mean square (RMS) roughness of 0.635 nm. A smooth thin-film surface was obtained using the sol-gel method.

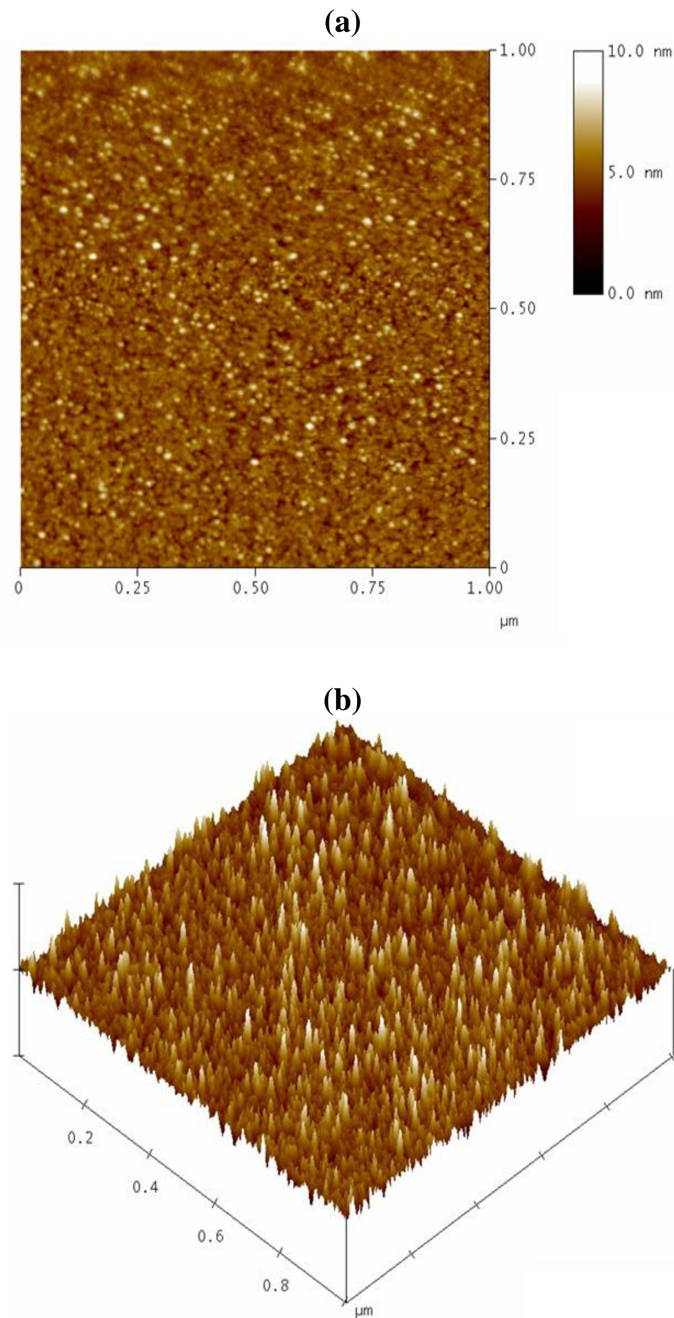

Figure 3. AFM images of the ZnO thin films annealed at 300℃, the scanning area of 1 μm^2 (a) RMS roughness analysis 0.635 nm and (b) Three-dimensional AFM image.

The AFM image of the Sn-doped ZnO thin-film is shown in Fig. 4. At Sn concentrations of 0.3 mole ratio, the root mean square (RMS) roughness was 0.375 nm. The surface of the un-doped ZnO was annealed at 300 ℃ (RMS = 0.635 nm), and was greater compared with Sn concentrations, which is 0.3 mole ratio (RMS = 0.375 nm). The addition of Sn improved the surface smoothness due to decreasing the grain size [14, 32]. These AFM results revealed that the Sn-doped ZnO thin-film showed good quality.

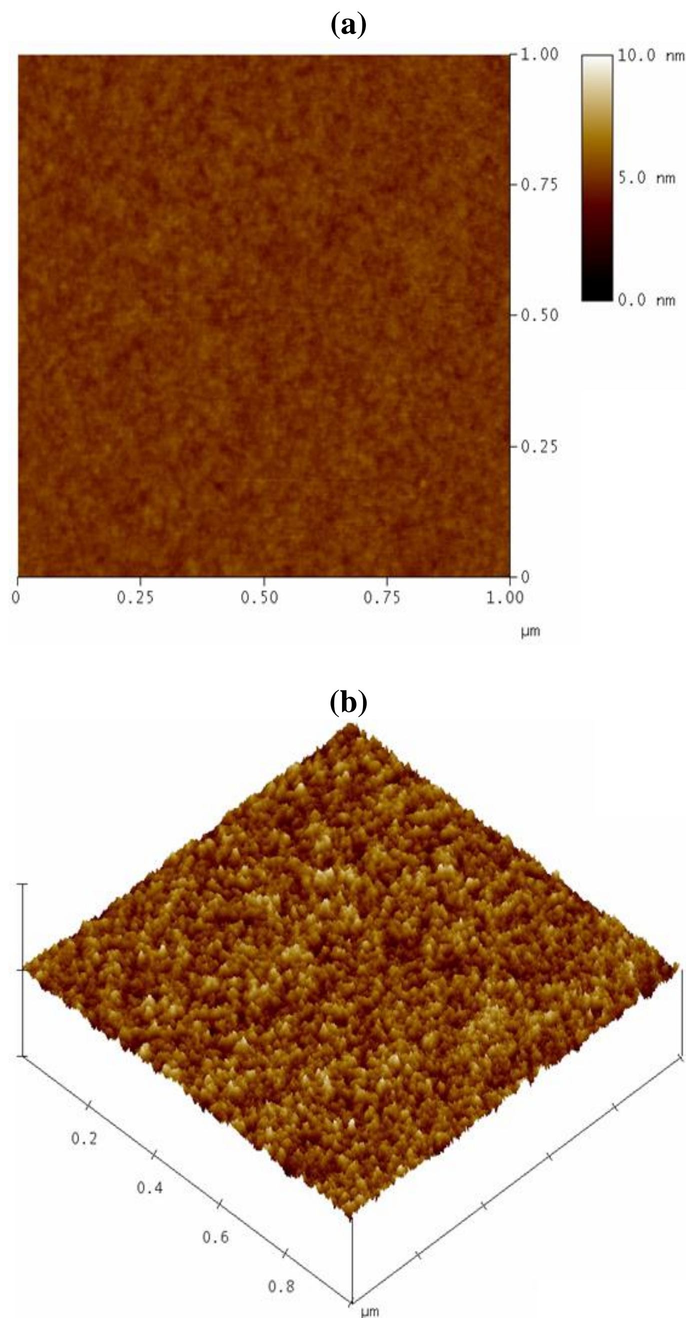

Figure 4. AFM images of the ZTO thin films (Sn concentrations of 0.3 mM) annealed at 300℃, the scanning area of 1 μm^2 (a) RMS roughness analysis 0.375 nm and (b) Three-dimensional AFM image.

The morphology of the ZnO/SiO_2 structures into an ultrathin film was observed by a field-emission TEM tool (JEOL JEM-2100F). In Fig. 5 shows cross-sectional TEM images of the ZnO/SiO_2 whose structures were annealed at 300 ℃[15]. Smooth and conformal interfaces were observed in the sample. The TEM images show that the structure by the sol-gel method resulted in an approximately 4.0 nm-thick ZnO film, which is a smooth semiconductor layer in the device. The surface morphology of the thin-film is crucial in a transistor.

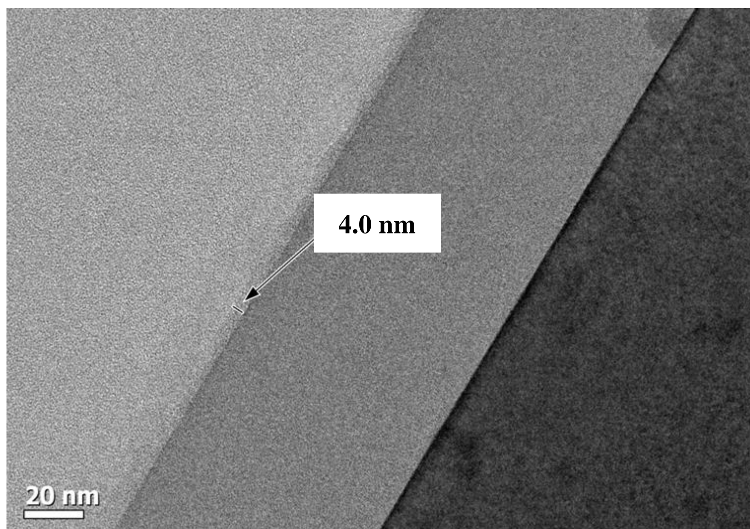

Figure 5. Cross-sectional TEM images of sol-gel-derived ZnO/SiO_2 structures annealed at 300℃ [15].

The morphology of the ZTO/SiO_2 structures into an ultrathin film was observed by a field-emission TEM tool (JEOL JEM-2100F). Fig. 6 shows a cross-sectional TEM image of the ZTO/SiO_2 whose structures were annealed at 300 ℃ with Sn concentrations of 0.3 mole ratio in ZTO thin-films. The amorphous nature of the approximately 4.5 nm-thick ZTO film was verified using TEM. Smooth and conformal interfaces were observed in the sample. The sol-gel method resulted in a smooth ZTO film.

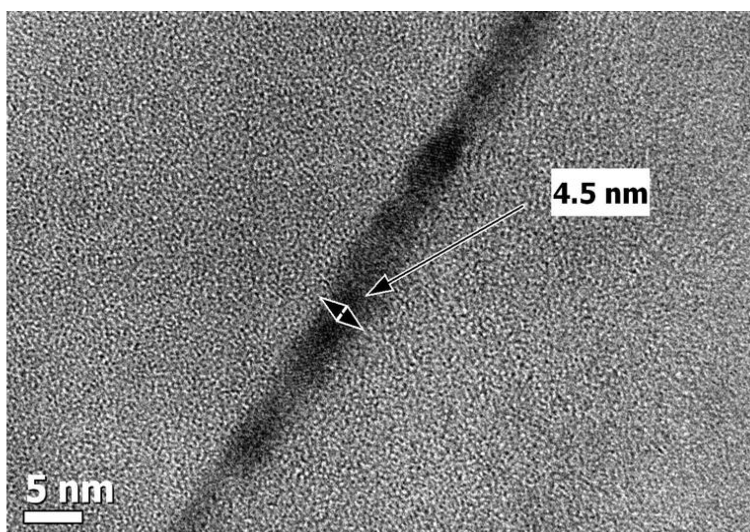

Figure 6. Cross-sectional TEM images of sol-gel-derived ZTO/SiO_2 structures of Sn concentrations of 0.3 mM and annealed at 300℃.

An Agilent 4156C analyzer was used to measure the drain current-gate voltage (I_D-V_G) transfer characteristic. Fig. 7 shows that at room temperature the drain current-gate voltage (I_D-V_G) transfer

characteristic curves of ZnO TFT that have a channel length of 70 μm and width of 2000 μm [15]. The ZnO TFT showed an on-off current ratio ($I_{on}/_{off}$) of up to nearly 10^5. The on-current (I_{on}) achieved can sustain as high as 3.81 × 10^{-6} A for V_D = 5 V, and the off-current (I_{off}) is as low as 2.18 × 10^{-11} A; the device has a field effect mobility (μ_{FE}) of 0.06 cm^2/V-s and a threshold voltage (V_{th}) of 15.6 V.

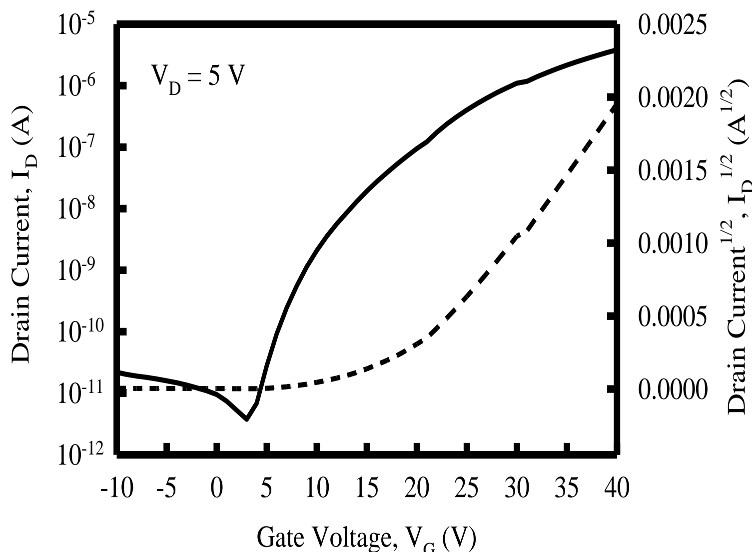

Figure 7. Transfer characteristics curves of ZnO TFT annealed at 300℃ by sol-gel method, V_D = 5 V [15].

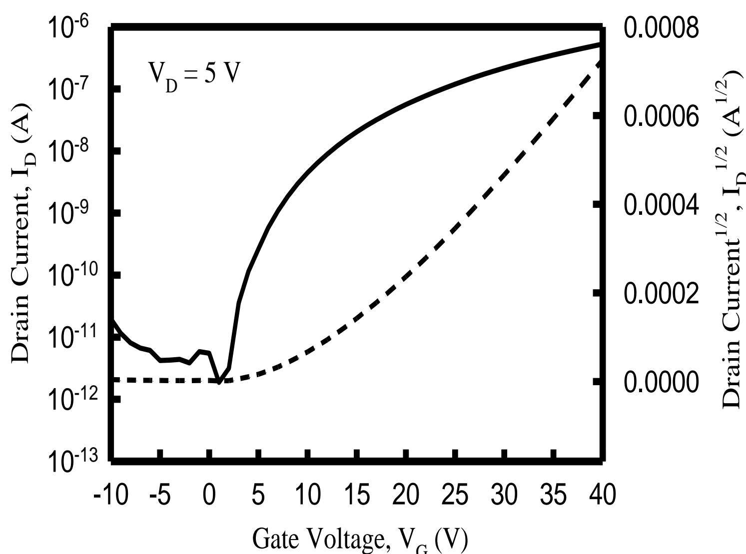

Figure 8. Transfer characteristics curves of ZTO TFT with Sn concentrations of 0.3 mM and annealed at 300 ℃ by sol-gel method, V_D = 5 V.

The drain current-gate voltage (I_D-V_G) transfer characteristic was measured using an Agilent 4156C analyzer. Fig. 8 shows the drain current (I_D) as a function of gate voltage (V_G) of the ZTO TFT

with Sn concentrations of 0.3 mole ratio. The V_D was fixed at 5 V, and V_G varied from -10 to 40 V. The drain current-gate voltage (I_D-V_G) transfer characteristics with Sn concentrations of 0.3 mole ratio showed that the on-off current ratio ($I_{on}/_{off}$) was 10^4 and the on current (I_{on}) was as high as 5.26×10^{-7} A. The threshold voltage (V_{th}) and field effect mobility (μ_{FE}) of the device were 5.6 V and 0.42×10^{-3} cm^2/V-s, respectively.

An Agilent 4156C analyzer was used to measure the drain current-gate voltage (I_D-V_G) transfer characteristic. Fig. 9 shows the I_D-V_G transfer characteristics for TFT based on ZnO (un-doped) and ZTO (0.3 mole ratio). The device performance parameters included the on current (I_{on}), off current (I_{off}), on-off current ratio ($I_{on}/_{off}$), threshold voltage (V_{th}), and field effect mobility (μ_{FE}). The TFTs operated as n-type channels in enhancement mode.

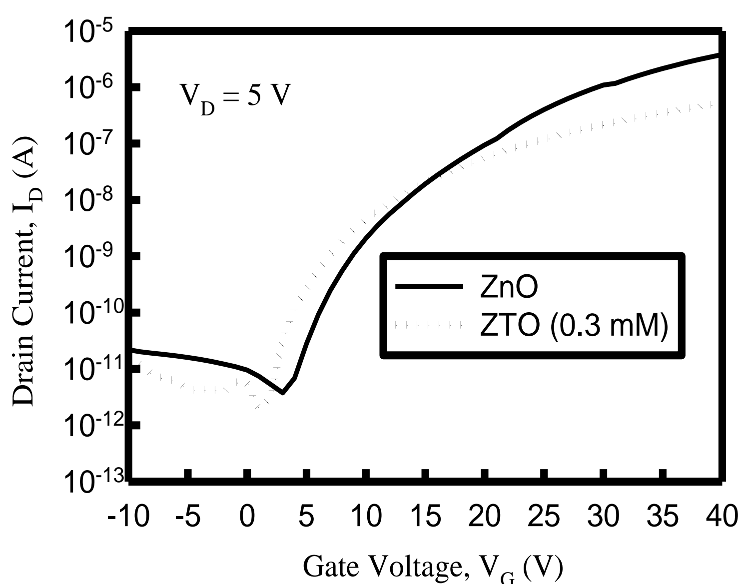

Figure 9. Transfer characteristics of TFT fabricated using ZTO channel annealed at 300℃ with different Sn concentrations ranging from 0 to 0.3mM, V_D = 5 V.

Table 1. Electrical performance parameters of transistors fabricated using a ZTO channel annealed at 300℃ with Sn/Zn mole ratio.

mole ratio of Sn : Zn	I_{on} (A)	I_{off} (A)	$I_{on/off}$	V_{th} (V)	μ_{FE} (cm^2/V-s)
0/1	3.81×10^{-6}	2.18×10^{-11}	10^5	15.6	60×10^{-3} [15]
0.3/1	5.26×10^{-7}	4.97×10^{-11}	10^4	5.6	0.42×10^{-3}

Electrical analysis showed that the field effect mobility (μ_{FE}) of these TFTs ranged between 0.42×10^{-3} and 60×10^{-3} cm^2/V-s, on-off current ratios ($I_{on}/_{off}$) were 10^4 - 10^5, and threshold voltages (V_{th}) were 5.6 - 15.6 V. These were compared with the un-doped ZnO TFT without an Sn component

annealed at 300 ℃. By reducing the Sn content, the on-off current ratio ($I_{on}/_{off}$) decreased from approximately 10^5 to 10^4, the threshold voltage (V_{th}) shifted from 15.6 to 5.6 V, and the field effect mobility (μ_{FE}) reduced from 60×10^{-3} to 0.42×10^{-3} cm^2/V-s, as shown in Table 1 [15]. The threshold voltage was derived as

$$V_{TN} = \frac{|Q'_{SD}(max)|}{C_{ox}} + V_{FB} + 2\phi_{fn} \quad (1)$$

where $Q'_{SD}(max)$, C_{ox}, V_{FB}, and $2\phi_{fn}$ are the maximal space charge density, gate oxide capacitance, flat band voltage, and potential difference between E_{Fi} and E_F in n-type, respectively. The carrier concentration was low when the low Sn^{+4} was low, which reduced the threshold voltage (V_{th}), as shown in (1). The low mobility can be attributed to grain boundary scattering caused by a less dense microstructure [32]. For the low Sn^{+4} content samples, the low mobility and low threshold voltage are the principal causes of the low current (I_{on}) and low on-off current ratio ($I_{on}/_{off}$) [15,31,33,34].

4. CONCLUSION

This paper presents a low cost and simple method to fabricate a ZnO TFT that is suitable for depositing onto an active channel layer of ZnO and ZTO using a sol-gel method. The ZnO TFT fabricated under low temperature (300 ℃) had an on-off current ratio ($I_{on}/_{off}$) of 10^5, field effect mobility (μ_{FE}) of 0.06 cm^2/V-s, and threshold voltage (V_{th}) of 15.6 V. The TFT was fabricated using the sol-gel method by coating the active channel layer of ZTO and annealing at 300 ℃; the threshold voltage (V_{th}) decreased to 5.6 V at Sn concentrations of 0.3 mole ratio. The ZnO and ZTO TFTs fabricated using the sol-gel method with a standard atmospheric pressure technique may be applied to next generation flexible electronics.

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