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Short Communication

Surface Texturization of Multicrystalline Silicon with Electrochemical Etching in NaOH/H_2O Solution for Solar Cell Application

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Preparation of the anti-reflective (AR) texture on crystalline silicon (c-Si) surface is an effective way to improve the c-Si solar cell performance. The surface texturization of multicrystalline silicon (mc-Si) is usually performed by chemical etching (CE) in HNO_3/HF/H_2O solution and the obtained surface reflectance (R) is normally higher than 20%. Here, a novel method based on electrochemical etching (ECE) in NaOH/H_2O solution was proposed for the surface texturization of mc-Si. Via the proposed alkaline ECE process, a macroporous texture with the pore feature size of about 100–200 nm could be prepared on the mc-Si wafer surface, reducing the weighted average surface reflectance (R_a) in a wide wavelength range of 400–1100 nm to be about 18.5%. To ensure the complete removal of the damaged layer on the mc-Si surface, the ECE process could be performed on mc-Si pretreated by the traditional CE process in HNO_3/HF/H_2O solution. Such two-step way resulted in a hierarchical texture with the macroporous structure superimposed onto micrometer-sized CE pits, which lowered the above R_a to be about 17.5% further. As a comparison, R_a was high up to 24.8% if only the traditional acidic CE process was carried out individually. The results indicated that such a novel ECE process in NaOH/H_2O solution had a great application potential to make the AR texture for the mc-Si solar cells.

Keywords: NaOH/H_2O solution; Electrochemical etching; Texturization; Multicrystalline silicon; Solar cell

1. INTRODUCTION

As an important way for renewable energy utilization, solar photovoltaic (PV) power is being paid more and more attention. Till now, crystalline silicon (c-Si) solar cells have always been dominating PV market with the market share of more than 90% [1]. To lower the cost of PV power generation, increasing the conversion efficiency and reducing the manufacture cost are critical for c-Si solar cells. The reduction of the optical loss is a first prerequisite for the solar cell to get high efficiency. For this, preparation of anti-reflective (AR) texture on the c-Si surface is a common way [2-4]. Additionally, multicrystalline silicon (mc-Si) is considered to have lower cost than monocrystalline silicon due to its casting process with low energy consumption [5, 6].

For monocrystalline silicon, the alkaline chemical etching (CE) in NaOH or KOH aqueous solution is usually used to prepare a texture with randomly distributed pyramids on the surface, which can lower the surface reflectance (*R*) to be about 10–12% [7, 8]. However, such method cannot be utilized on mc-Si, since plenty of grains with different orientations on mc-Si surface present different anisotropic etching behaviors in the alkaline etching solution, which can lead to an obvious color difference on the surface due to different *R* obtained on different grains. As a result, the texturization of mc-Si has to adopt the acidic CE process in $HNO_3/HF/H_2O$ solution traditionally [9, 10]. The acidic etching is isotropic, resulting in a texture with oval-like pits in micrometers. However, the obtained surface *R* is much higher than that of the pyramidal texture since the pit morphology has a relatively low aspect ratio. More importantly, for the wafer fabrication, the traditional slurry wire slicing (SWS) is nowadays being replaced by the diamond wire slicing (DWS). DWS possesses many advantages such as high throughput, low kerf loss and low operation cost. However, for $HNO_3/HF/H_2O$ CE process, it becomes difficult to prepare good texture on the mc-Si wafers produced by DWS since the DWS process makes the damaged layer thinner on the wafer surface. The thick damaged layer on SWS mc-Si wafers can promote the acidic CE process by providing lots of defects as the initial etching sites.

In order to reduce the surface *R* of mc-Si further, some alternative dry or wet etching technologies are emerging. The dry etching methods mainly include reactive ion etching (RIE) and laser etching. RIE can prepare a texture with high aspect ratio via physical bombardment from high-energy ions together with chemical etching from reactive radicals [11, 12]. However, the vacuum equipment utilized for RIE is expensive and some toxic gases such as SF_6 have to be adopted. Laser etching can change the c-Si surface by melting Si with high-energy photons [13]. The accuracy of laser etching is high, but the laser itself is expensive and the etching rate is low. Metal catalyzed chemical etching (MCCE) and electrochemical etching (ECE) are representatives for wet etching methods. During the MCCE process, the etching is carried out in a HF aqueous solution containing some oxidants such as H_2O_2 with some noble metal particles as the catalysts on mc-Si surface. During the etching, the metal particles will sink gradually and result in a porous structure finally. After the etching, a metal removal step has to be adopted [14-16]. In general, MCCE is relatively complex. Its process window is narrow and the reaction condition has to be controlled strictly. The ECE method is usually performed in a HF aqueous solution. When a certain bias voltage is applied onto the c-Si wafer, which is utilized as the anode, the c-Si surface can be oxidized and etched by HF selectively. As a result, a porous structure will also be formed on the c-Si surface [17-19]. We have ever fabricated porous silicon by combining the MCCE and ECE together [20]. Nevertheless, the ECE method has to be modified further due to the high harm risk of HF solution.

Thus, it is still very significant to develop a low-cost and safe texturization method suitable for mc-Si to obtain a lower surface *R*. To realize this, a new texturization process via the anodic oxidation of mc-Si by the alkaline ECE treatment in $NaOH/H_2O$ solution was proposed here.

2. EXPERIMENTAL

The original mc-Si wafer was commercially available DWS solar-grade p-type mc-Si with the resistivity of 1.0~3.0 Ω·cm and the thickness of about 180 μm.

As a control, the mc-Si wafer was treated by the traditional CE process in $HNO_3/HF/H_2O$ solution. HF(50wt%) and HNO_3(75wt%) were utilized with the $HNO_3:HF:H_2O$ volume ratio of about 6:3:4. To improve the texturization performance, a specific industrial additive was incorporated into the solution with the amount of about 1.0 vol%. The CE process was carried out at room temperature for about 2 min. Then, a mild etching of 5 wt% NaOH aqueous solution was utilized to smoothen the nanoporous feature on the obtained oval-like texture.

The ECE process on the mc-Si wafer was performed in an electrochemical etching bath with two electrodes setup. The mc-Si was utilized as the anode by attaching onto a copper electrode firmly. Another copper electrode was adopted as the cathode. 0.3 M $NaOH/H_2O$ solution was utilized as the electrolyte in the electrochemical bath. An adjustable bias voltage was applied onto the electrodes via the power supply to keep the etching current stable at about 28 mA/cm^2. The ECE process was performed at room temperature. A magnetic stirring was adopted to maintain the solution temperature constant during the whole etching period, which was fixed as 30 min.

In order to ensure the complete removal of the damaged layer on the mc-Si surface, a two-step way with the alkaline ECE process performed following the traditional acidic CE process was also demonstrated.

After all the texturization processes, the textured wafers were rinsed with the deionized (DI) water completely, followed by N_2 blow drying. Then, for characterization, Sigma, Carl Zeiss scanning electron microscope (SEM) was adopted to observe the wafer surface and cross-sectional morphologies. The surface reflectance (R) in the wavelength range of 300–1200 nm was measured on QEX7 tester from PV Measurement. Further, the weighted average surface reflectance (R_a) in the wavelength range of 400–1100 nm was calculated according to the equation (1):

$$R_a = \frac{\int_{\lambda_1}^{\lambda_2} R(\lambda)\times n(\lambda)d\lambda}{\int_{\lambda_1}^{\lambda_2} n(\lambda)d\lambda} \quad (1)$$

where, $n(\lambda)$ and $R(\lambda)$ represent the photon number and the reflectance for the light with wavelength λ in the sun spectrum of AM1.5G. λ_1 and λ_2 are 400 nm and 1100 nm, respectively. d is the derivative operator.

3. RESULTS AND DISCUSSION

Figure 1 gives out the original surface morphology of the utilized mc-Si wafer before the texturization treatment. The as-cut DWS mc-Si wafer presents a relatively flat surface with obvious parallel cutting scratches corresponding to the damaged layer resulted from the DWS process. The morphology is obviously different from that of SWS wafer [21]. The damaged layer on DWS wafer is relatively thin with a small surface roughness, which can weaken the etching effect of the acidic CE process in $HNO_3/HF/H_2O$ solution.

When the alkaline ECE process in $NaOH/H_2O$ solution was applied onto the mc-Si wafer, the electrochemical oxidation of silicon can be expressed as follows [22]:

Cathodic reaction: $4H_2O + 4e^- \rightarrow 4OH^- + 2H_2\uparrow$ (2)

Anodic reaction: $Si + 4OH^- + 4h^+ \rightarrow Si(OH)_4$ (3a)

or $Si + 4OH^- + 4h^+ \rightarrow SiO_2 + 2H_2O$ (3b)

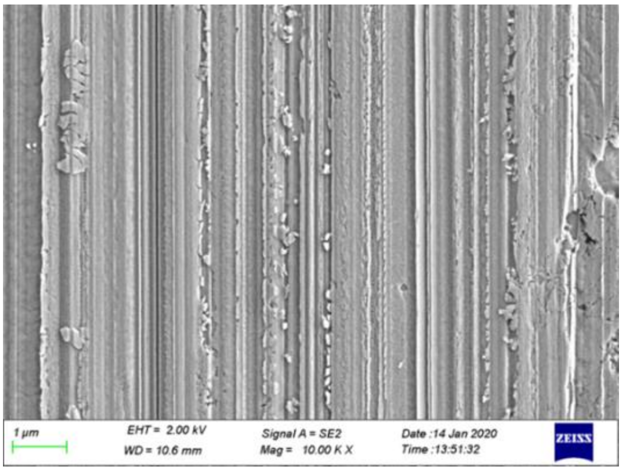
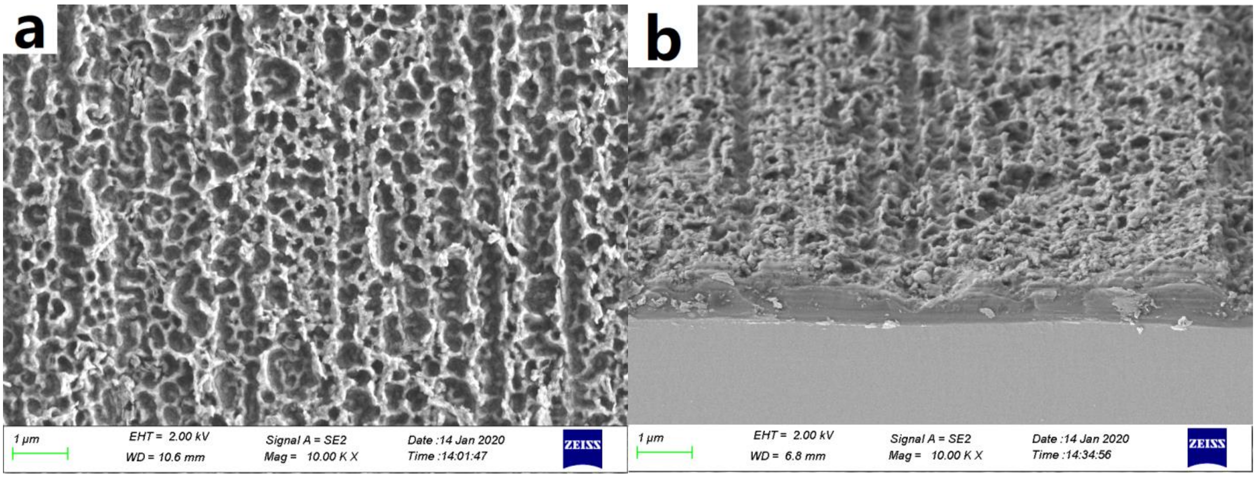


Figure 1. The original surface morphology of the as-cut diamond wire sliced (DWS) multicrystalline silicon (mc-Si) wafer.

On the anode, the surface Si atoms are attacked by the OH^- groups and the oxidation occurs at the active anodic sites. When the oxidation reaction is mild, the oxidation product of silicon is a soluble silicate, i.e. $Si(OH)_4$, as shown in reaction (3a). While the silicate diffuses from the Si surface to the solution, the Si oxidation can be performed continuously, which results in the Si etching. When the oxidation rate is faster than the diffusion rate of the oxidation product if the applied bias voltage is high, a passivation oxide film will be formed at the silicon surface as indicated by reaction (3b). Once the oxide film is formed, the current will decrease greatly and the Si oxidation rate will also be reduced. The oxide will grow thick more and more, which will make it difficult for the OH^- groups to diffuse onto the Si surface.



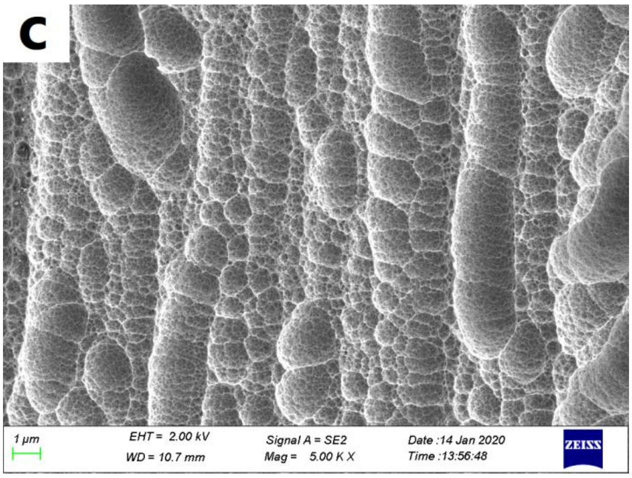


Figure 2. The textured morphology obtained on the diamond wire sliced (DWS) multicrystalline silicon (mc-Si) wafer. (a) surface morphology and (b) cross-sectional morphology obtained by the electrochemical etching (ECE) process in NaOH/H_2O solution, and (c) surface morphology obtained by the traditional chemical etching (CE) in HNO_3/HF/H_2O solution.

So the oxidation reaction will decelerate further although the grown oxide can also be etched back by the alkaline solution slowly. The oxidation reaction is highly dependent on the electrical field distribution on the Si/solution interface, which indicates that the oxidized and etched degree is unequal obviously on different sites, leading to the formation of a macroporous structure finally.

The obtained macroporous morphologies are as shown in Fig.2 (a) and (b). For a comparison, the texture prepared by the traditional CE process in HNO_3/HF/H_2O solution is also presented in Fig.2 (c). It can be seen that the morphology obtained by the novel alkaline ECE process is obviously different from that obtained by the traditional acidic CE process.

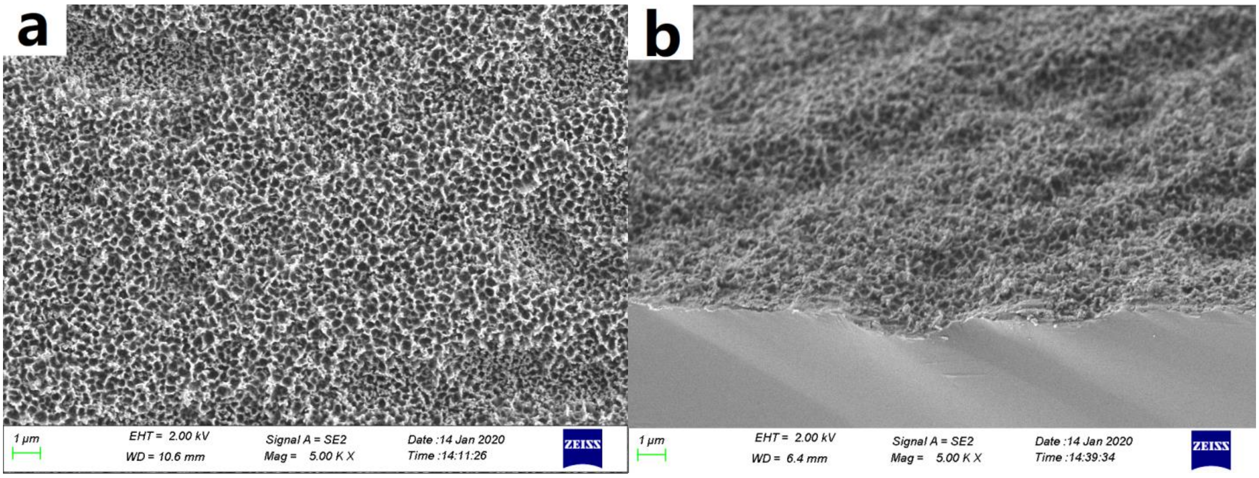


Figure 3. The textured morphology obtained on the diamond wire sliced (DWS) multicrystalline silicon (mc-Si) wafer by a two-step way with the alkaline electrochemical etching (ECE) following the acidic chemical etching (CE). (a) surface morphology and (b) cross-sectional morphology.

Via the ECE process, a macroporous structure with the feature size of the etched pores as about 100-200 nm is prepared. The remained silicon wall between the adjacent pores is very thin. However, the traditional CE process results in shallow oval-like pits with the size in several micrometers. As a result, the obtained macroporous structure by the alkaline ECE process demonstrates a higher aspect ratio than the pits obtained by the acidic CE process. Nevertheless, due to the nano-scale feature of the macroporous structure, the damaged layer might be remained partially on the mc-Si surface while the ECE process is finished. To avoid this, a two-step way by performing the alkaline ECE process following the acidic CE process was carried out. As shown in Fig. 3, the two-step way leads to a hierarchical texture with the macroporous feature superimposed onto the micrometer-sized CE pits.

The different textures should demonstrate different AR performance. Fig. 4 gives out the surface R spectra on the obtained textured surfaces. The weighted average surface reflectance (R_a) in the wavelength range of 400–1100 nm was further calculated. Via the traditional acidic CE process in $HNO_3/HF/H_2O$, the obtained R_a is about 24.8%, which indicates that the AR performance is not good. Surprisingly, R_a is lowered to be about 18.5% by the alkaline ECE process. Via the two-step way combining the alkaline ECE with the acidic CE together, R_a further decreases to be about 17.5%. The AR performance is improved greatly due to the nano-scale feature of the macroporous structure. So although the alkaline ECE process proposed here is still not optimized, it has demonstrated better performance to fabricate the AR texture on DWS mc-Si wafer than the traditional $HNO_3/HF/H_2O$ etching. It also presents some advantages, comparing to the traditional anodic oxidation of silicon in HF contained solution. Salman et al. fabricated porous silicon on p-type c-Si wafer by the ECE process in the solution of $HF:C_2H_5OH$ (1:4). Pores with sphere-like appearance and thick walls were found to be randomly distributed with the size in very little nano-scale and the length of several tens of micrometers [23]. Liu et al. reviewed the ECE process in HF contained solution as one way to fabricate black silicon. It was concluded that the resulted pore morphologies depended on the wafer doping type and dopant concentration. For p-type Si, the pore size was usually in the range of 1 to 100 nm [24]. And with the increase of the etching time or the etching current, the generated pore would extend into the c-Si wafer deeply, resulting in a thick porous layer, which was however incompatible with the solar cell bearing a junction depth of only 350 nm, since the porous layer itself might absorb and hence waste a substantial amount of light [25]. Obviously, the porous silicon obtained here by the ECE in $NaOH/H_2O$ solution could not meet with these problems for the solar cell application due to its relatively large size and shallow depth.

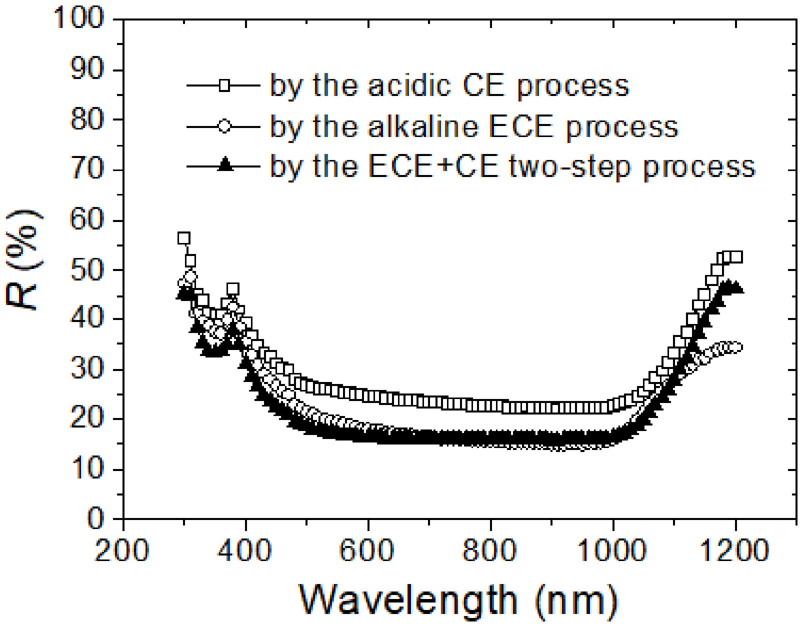


Figure 4. The textured surface reflectance (*R*) of the diamond wire sliced (DWS) multicrystalline silicon (mc-Si) wafers obtained by the chemical etching (CE) in $HNO_3/HF/H_2O$ solution, the electrochemical etching (ECE) in $NaOH/H_2O$ solution and the two-step etching process of the ECE and CE combination, respectively.

Next, it should be considered how to integrate such excellent AR texture obtained by the alkaline ECE process onto a real mc-Si solar cell. The macroporous structure prepared by the ECE process is not compatible with the secondary cleaning process of the solar cell fabrication, where a dilute HF aqueous solution will be utilized to etch off the phosphorus silicon glass generated during the emitter-forming diffusion. If the ECE process is carried out before the diffusion process, the formed macroporous structure is easy to be oxidized and to be incorporated with lots of phosphorus atoms. That is, the macroporous structure will be changed into the phosphorus silicon glass. It can be etched off by the subsequent HF cleaning. Hence, to avoid this, the ECE process can be carried out after the secondary cleaning process. Besides keeping the excellent AR performance, this way will also bring another benefit that the macroporous structure may demonstrate a certain degree of surface passivation performance due to its anodic oxidation product in nature. In fact, such strategy has been applied to fabricate mc-Si even monocrystalline silicon solar cells with porous silicon emitter [26-28], where the porous silicon structures were prepared by the ECE process in HF solution or MCCE process. Obviously, for the alkaline ECE process in $NaOH/H_2O$ solution here, comparing to the traditional CE process in $HNO_3/HF/H_2O$ and the ECE process in HF contained solution, it is much safer without the hazardous HF and nitrogen-contained products released, comparing to the RIE or laser etching, it is much cheaper without the requirement for expensive equipment, and comparing to the MCCE process, it is much easier to perform without the metal catalyst deposition and removal steps. Additionally, other alkali agents can also be utilized, such as KOH, Tetramethylammonium hydroxide (TMAH) and so on, which will give the alkaline ECE process much wider availability.

4. CONCLUSIONS

A novel method based on electrochemical etching (ECE) in NaOH/H_2O solution was proposed for the surface texturization of mc-Si. By the mentioned ECE process, a macroporous texture with the pore feature size of about 100–200 nm was prepared, reducing the weighted average surface reflectance (R_a) in a wide wavelength range of 400–1100 nm to be about 18.5%. When the ECE process was performed following the traditional chemical etching (CE) process in HNO_3/HF/H_2O solution, a hierarchical texture with the macroporous structure superimposed onto micrometer-sized CE pits was formed further. As a result, the above R_a was lowered to be about 17.5%. The AR performance was improved greatly due to the nano-scale feature of the macroporous structure. As a comparison, R_a was high up to 24.8% if only the traditional HNO_3/HF/H_2O CE process was carried out. Additionally, comparing to the current texturization methods, such ECE process could be performed easily without the hazardous HF and nitrogen contained products released. The results indicate that the novel alkaline ECE process in NaOH/H_2O solution has a great application potential to make the AR texture in the mc-Si solar cell fabrication.

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