# Facile Electroless Deposition of Zinc Oxide Ultrathin Film for Zinc Acetate Solution-processed Transistors

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A low-cost, ultra-thin, transparency and high-quality zinc oxide (ZnO) film was successfully demonstrated as the carrier transporting and semiconducting layer for thin-film transistor (TFT) devices. The ZnO ultra-thin film with 3.7 nm in thickness was spin-coated from zinc acetate sol-gel solution under electroless condition. The film structure was characterized by atomic force microscopy and x-ray diffraction spectroscopy, respectively. Among various processing temperatures, the electrical property of the fabricated TFT verified the devices could be successfully achieved from suitable annealing temperature of 300 to 700 °C. However, the higher treatment temperature of 800 to 900 °C deteriorated the transistor property due to the loss of oxygen vacancy. The electrical properties of these ZnO-based n-type TFTs were obtained as follows: the mobility ($\mu_{sat}$) ranged from 0.47 to 1.78 cm$^2$ V$^{-1}$ s$^{-1}$, the on/off current ratio ranged from $5.7 \times 10^5$ to $1.6 \times 10^6$, and the threshold voltage ranged from 9.7 to 17.3 V. The long-term (100 days) characterization for the evaluation of the ultra-thin ZnO TFT reliability on the mobility and on/off current ratio strongly suggested the effectiveness of solution-processed ultra-thin film transistors. This proposed efficient sol-gel solution method to fabricate transparent ZnO ultra-thin film was relatively simple and cost-effective technique, and could be used as a new candidate of material for next-generation electronic devices to meet the growing demand of small feature bioelectronic sensor, light emitting diode and flexible panel.

**Keywords:** Ultra-thin film, zinc oxide, sol-gel solution, thin-film transistor, long-term reliability

## 1. INTRODUCTION

Electronic devices such as thin-film capacitor, electrolyte-insulator-semiconductor, nanowire field-effect transistor and nanobelt field-effect transistor can be used for future technologies of

bioelectronic sensor, small feature thin-film transistor (TFT), light emitting diode and flexible panel [1-5]. Among them, low-cost metal-oxide materials present an alternative opportunity for transparent semiconducting active layers to fabricate transparent devices. Transparent metal-oxide semiconductors (TMOSs) have many advantages, such as transparency in the visible region due to their large bandgap, environmental stability, non-toxicity and high mobility. In contrast to oxide-free material (for example, GaN), metal-oxide materials can be easily prepared from low-cost sol-gel solution to deposit thin film for device purpose [6,7]. ZnO, one of TMOSs, has been reported for transparent active-channel materials in TFTs [5]. However, such device [8,9] from ZnO thin film preparation always requires a relatively thick ZnO film (thickness > 60 nm). Hence, the thicker ZnO film increases the fabrication cost and reduces the transparency of such devices. As shrinking the ZnO thickness, the reliability issue always restricts the development of ZnO-based TFT. How to fabricate an actually reliable thin ZnO film (thickness < 20 nm) is still a challenge issue for transparent semiconductor towards shrinkage device to meet future high functionality. Moreover, the transparent devices with less than 20-nm ZnO film should demonstrate better transparency and low cost of film fabrication for further product application.

Many physical and chemical techniques such as chemical vapor deposition [10], voltage deposition [11], spray pyrolysis [12], sputtering [13,14], evaporation [15], laser ablation [16] and sol-gel solution method [17] are reported to deposit ZnO thin films at thickness higher than 60 nm. To the best of our knowledge, no literature mentions the reliable device can be fabricated from ultra-thin ZnO semiconductor film at less than 10 nm. This ultra-thin thickness can guarantee the sufficient transparency and low-cost fabrication. Solution-derived thin-film deposition methods could offer many advantages such as simplicity, low chemical cost, and high throughput that enable the future fabrication of high-performance and low-cost electronics devices. In addition, the sol-gel solution-derived deposition method can be operated in the normal pressure environment instead of expensive high-vacuum system.

Among various II-VI group materials, intrinsic n-type semiconducting devices based on ZnO thin film offer a promising alternate for amorphous silicon film due to safety issue, availability and comparable mobility. The change of electrical conductivity of ZnO thin film based device is mainly due to oxygen vacancies and/or zinc interstitials. Some reports have mentioned on the preparation of p-type ZnO films from suitable doping [8,9]. The poor electrical and dope-required property limits the practical application of p-type ZnO. In comparison with p-type ZnO material, the n-type ZnO semiconductor thin film has gained more interest due to its unique undoped and excellent electrical properties.

The primary aim of this work is to study the fabrication of ultra-thin 3.7-nm ZnO films only from zinc acetate sol-gel solution under electroless environment and its impact on the electronic properties for thin-film transistors. A series of ZnO films are formed at different annealing temperatures. The film nanostructure is investigated by using a wide range of characterization techniques such as atomic force microscope (AFM), X-ray diffraction (XRD) and transmission electron microscope (TEM). In addition, the saturation mobility ($\mu_{sat}$), on/off current ratio, and threshold voltage of the ultra-thin n-type ZnO transistor with respect to long-term reliability is carefully investigated from bottom-gate and top-contact transistor architecture.

## 2. EXPERIMENTAL DETAILS

### 2.1 Preparation and deposition of ZnO materials

The 0.05 M zinc acetate solution was prepared by dissolving zinc acetate dihydrate [$Zn(CH_3COO)_2 \cdot 2H_2O$] into 2-methoxyethanol. Prior to spin-coating, the formulated solution was rigorously stirred for at least 2 hour under room temperature and filtered through 0.2 μm membrane filters. Prior to the spin-coating process, the silicon substrate was treated with $O_2$ plasma for 1 minute in oxygen plasma reactor (Harrick Scientific Corp.); which tool supplied a plasma power of 18 W. The zinc acetate sol-gel solution was spin coated on silicon wafer at a speed of 500 rpm for 30 s and then 1000 rpm for 30 s. Fig. 1 displays the chemical transformation, the hydrolysis and condensation reactions for this sol-gel reaction. After two-step spin-coating process, these films were treated with annealing temperatures from 300 to 700 °C, respectively. The surface morphology of the ZnO thin films over silicon wafer was evaluated by using AFM (Digital Instruments Nanoscope, D-5000) under 1 μm × 1 μm scan size and 1 Hz scan rate. XRD pattern of the fabricated film was obtained from Cu K$\alpha$ radiation by using a Rigaku D/max-IIIB diffractometer. The thickness of ZnO ultra-thin film was measured by TEM image analysis. The preparation, deposition and further device fabrication was depicted schematically in Fig. 2. All chemicals were used without further purification.
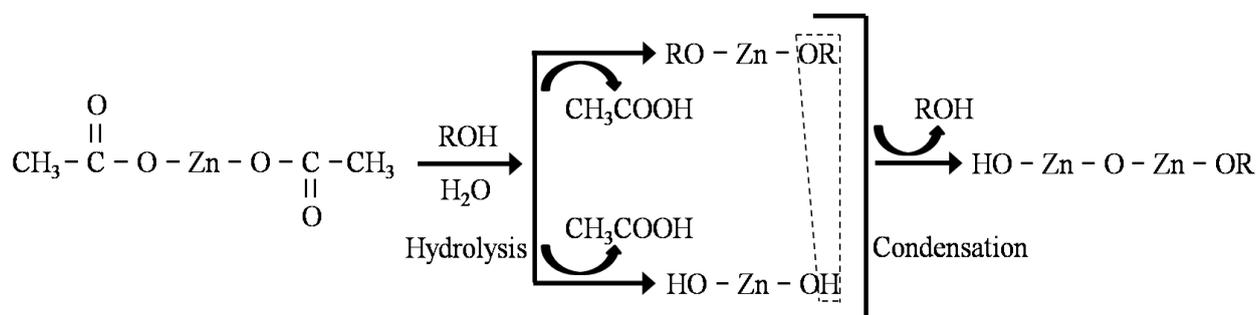


**Figure 1.** Schematic representation of zinc acetate sol-gel reaction.

### 2.2 Device fabrication and characterization

Firstly, standard RCA clean was applied to remove surface particles and other contaminations on p-type silicon wafer. The 100 nm-thick $SiO_2$ as gate dielectric layer was deposited on p-type silicon wafer by using horizontal furnace. The fabrication of sol-gel solution-derived thin-film transistor with ultra-thin ZnO active channel was also illustrated in Fig. 2. The zinc acetate sol-gel solution to form the active channels was subject to spin-coating. In order to obtain a crack-free, uniform and smooth film, the concentration of zinc acetate sol-gel solution was carefully optimized. Prior to the succeeding electrode formation, a shadow mask was covered onto the film of interest. After thermal evaporation of Al pattern under high vacuum ($10^{-6}$ mbar) and removal of the shadow mask, the 300-nm-thick Al source and drain electrodes were formed. The channel length (L) and width (W) between Al electrodes were 70 and 2000 μm, respectively. Similarly, the 300-nm-thick Al gate electrodes, on the backside of

substrate, were also deposited by thermal evaporator. Electrical measurement of ZnO TFT device was performed by using an Agilent 4156 probe station.

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┌─────────────────────┐        ┌─────────────────────┐
│ Zinc acetate dihydrate│        │   Prime p-type      │
│          +          │        │      wafer          │
│   2-methoxyethanol  │        │                     │
└─────────────────────┘        └─────────────────────┘
           │                              │
           ▼                              ▼
┌─────────────────────┐        ┌─────────────────────┐
│   0.05 M ZnO        │        │   Wet oxide         │
│   solution          │        │   (100 nm)          │
└─────────────────────┘        └─────────────────────┘
           │                              │
           └──────────────┬───────────────┘
                          │ Spin-coating
                          ▼
                ┌─────────────────────┐
                │   ZnO thin film     │
                │   deposition        │
                └─────────────────────┘
                          │ Annealing 100 ~ 900 ℃
                          ▼
                ┌─────────────────────┐
                │  Source and drain   │
                │  deposition         │
                └─────────────────────┘
                          │
                          ▼
                ┌─────────────────────┐
                │   Bottom gate       │
                │   deposition        │
                └─────────────────────┘
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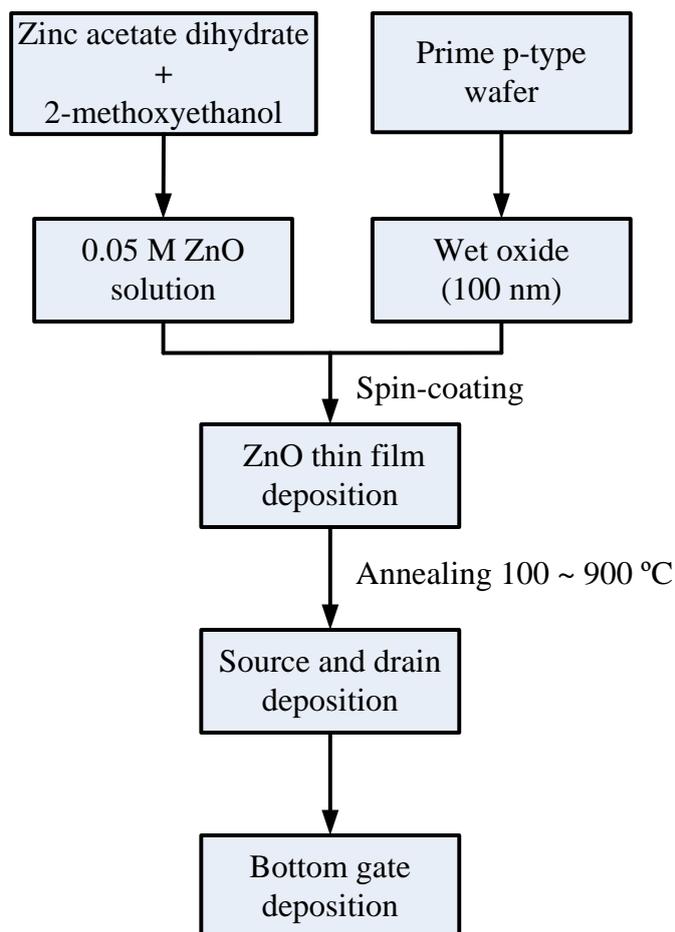
**Figure 2.** The process flow of the sol-gel solution-derived ZnO TFTs.

## 3. RESULTS AND DISCUSSION

*3.1 Ultra-thin thickness, transparency and smoothness of the proposed ZnO film*

The quality of an interface between an insulator and a semiconductor layer are extremely crucial for practical device fabrication and operating reliability. Fig. 3a illustrates the bottom-gate and top-contact design for n-type ZnO TFT devices. As mentioned above, the transparent semiconductor layer of ultra-thin ZnO film is fabricated by low-cost zinc acetate solution-processed method. Fig. 3b shows cross-sectional TEM image of the $ZnO/SiO_2$ structures annealed at 300 °C. The TEM image indicates that the sol-gel solution-derived semiconductor layer consists of only 3.7-nm-thick ZnO film which acts as an active semiconductor layer in TFT device. We will verify this film has high quality on transistor property in the latter section. In order to confirm the fully transparency of this film, we deposit the ultra-thin ZnO film onto glass and put the glass on our university logo. Fig. 3c

demonstrates the transparent property of the deposited ZnO thin film on glass. In comparison with the un-coated ZnO glass sample, the transmittance remains very high after ZnO deposition and is measured > 99.5% at visible light range (400 to 820 nm).

All the films are grown by low cost spin-coating method and annealed at respective temperatures from 300 to 700 °C. In general, all the surface roughness of AFM image in Fig. 4a-e is less than 1 nm and reveals that the proposed transparent ZnO ultra-thin film has good large area quality, smoothness, crack-free morphology and uniform surface. We compare all the temperature induced surface roughness effect in Fig. 4f. Interestingly, the 300 °C annealing has exceptional low roughness of 0.38 nm. However, the roughness gradually increases with annealing temperature from 0.64 nm to 0.76 nm for temperature range of 400-700 °C. The application of such transparent ultra-thin film for future flexible electronic product is required low temperature process (i.e. < 350 °C), and this study also support the lowest annealing temperature of 300 °C can create the most smoothness film. This observation is beneficial for using this smooth film to fabricate transistor device for future practical application. What is the decisive reason on ZnO ultra-thin film for increasing surface roughness with annealing temperature? This observation on roughness could be ascribed to the fact that the primary ZnO crystallites aggregate to larger secondary particles minority when the temperature is increased. Since the prediction of AFM images of films from Fig. 4a-e, the grain size also increases with annealing temperature up to 700 °C. Previous reports also support this finding [18,19].
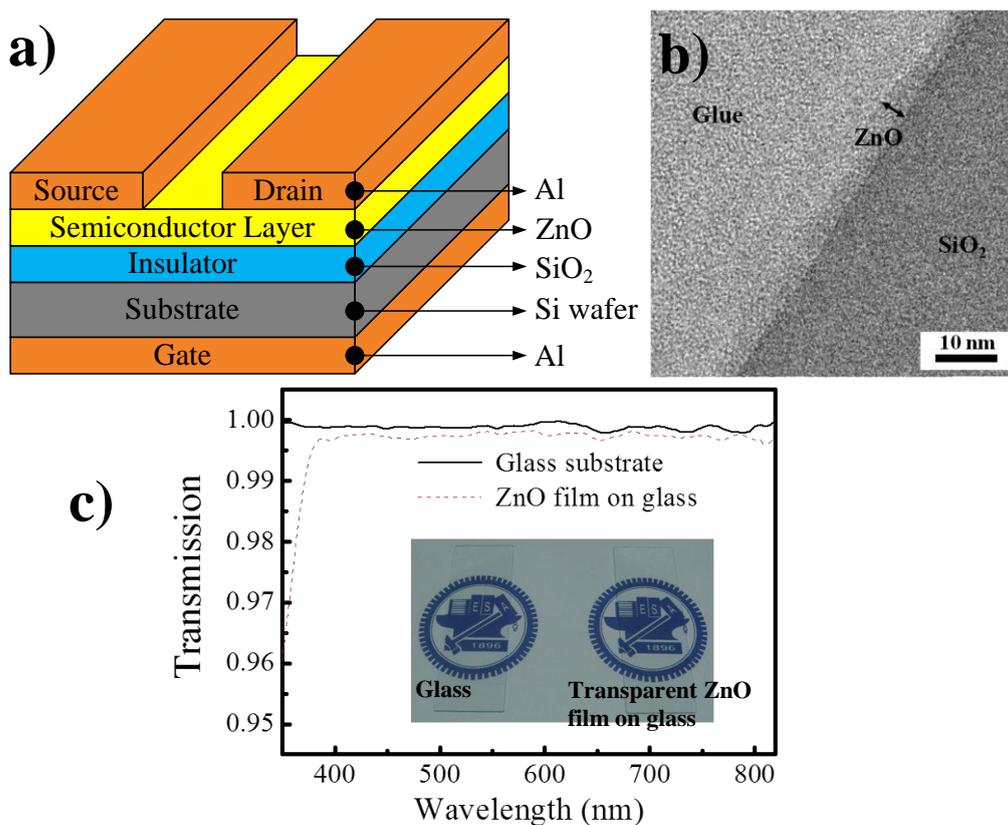


**Figure 3.** a) A schematic structure of the ZnO thin-film transistor. b) Cross-sectional TEM images of ZnO layer annealed at low temperature of 300°C. c) Transmission spectra of glass substrate and

transparent ultra-thin ZnO film onto glass. Inset: the ZnO film onto glass and put the glass over our university logo.
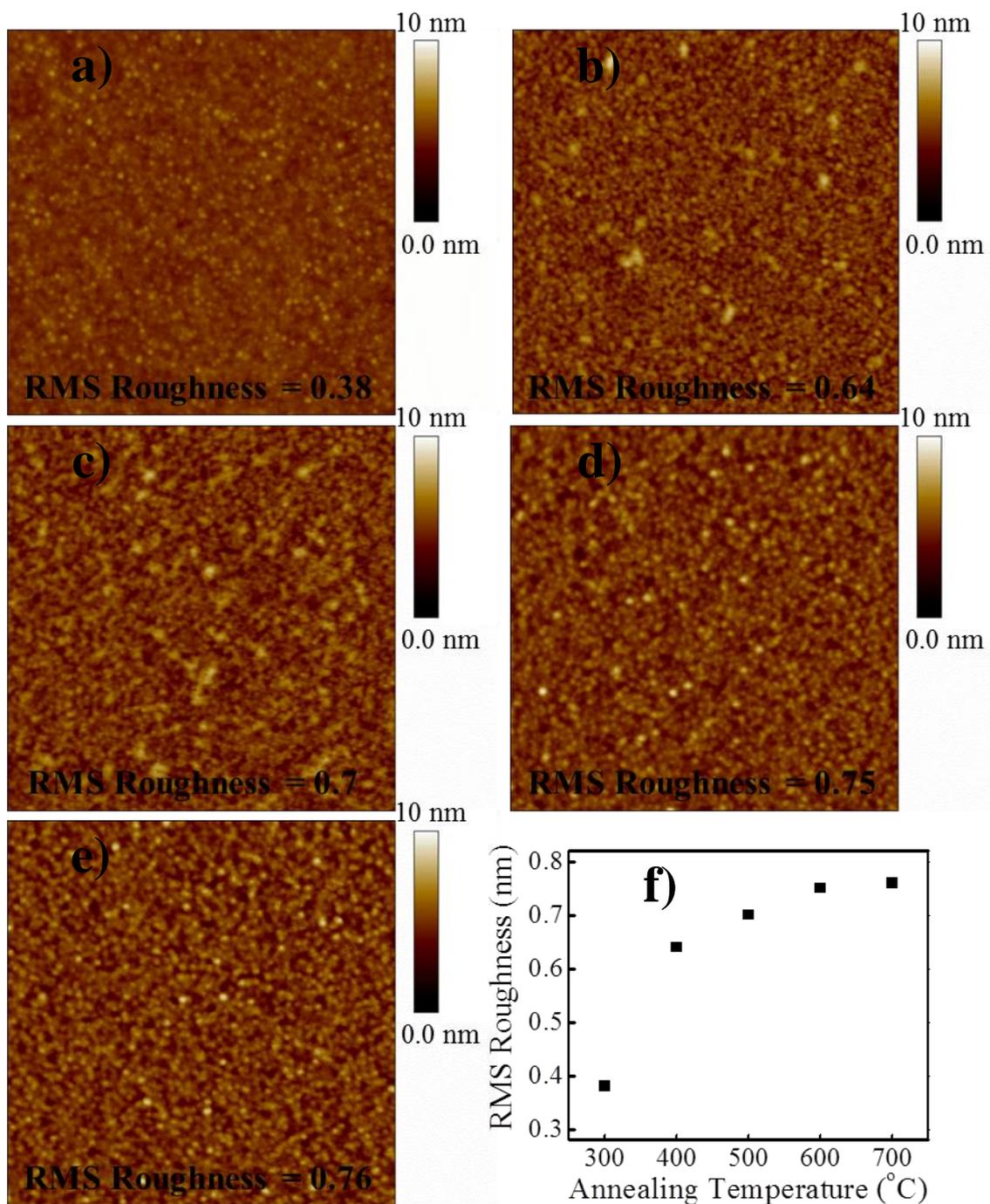


**Figure 4.** AFM images (scale: 1μm × 1μm) of the ultra-thin ZnO films annealed at a) 300 °C, b) 400 °C, c) 500 °C, d) 600 °C, and e) 700 °C. f) RMS roughness of ZnO surface as a function of temperature.

*3.2 Identification of the phase structure of various ZnO films from XRD Analysis*

The identification of the phase structure of ZnO films is investigated by XRD analysis and the results are illustrated in Fig. 5. XRD spectra in Fig. 5 are represented for ultra-thin ZnO films annealed

at 300 °C, 400 °C, 500 °C, 600 °C and 700 °C, respectively. On a microscopic scale, however, the ZnO film consist of amorphous phase as there are no resultant diffraction peaks observed when we anneal the sample at 300 °C. Interestingly, the XRD patterns are seen for all the films after the annealing processing of 400-700 °C and have three peaks, which correspond to (100), (002), and (101) diffractions at 31.7°, 34.5°and 36.5°.
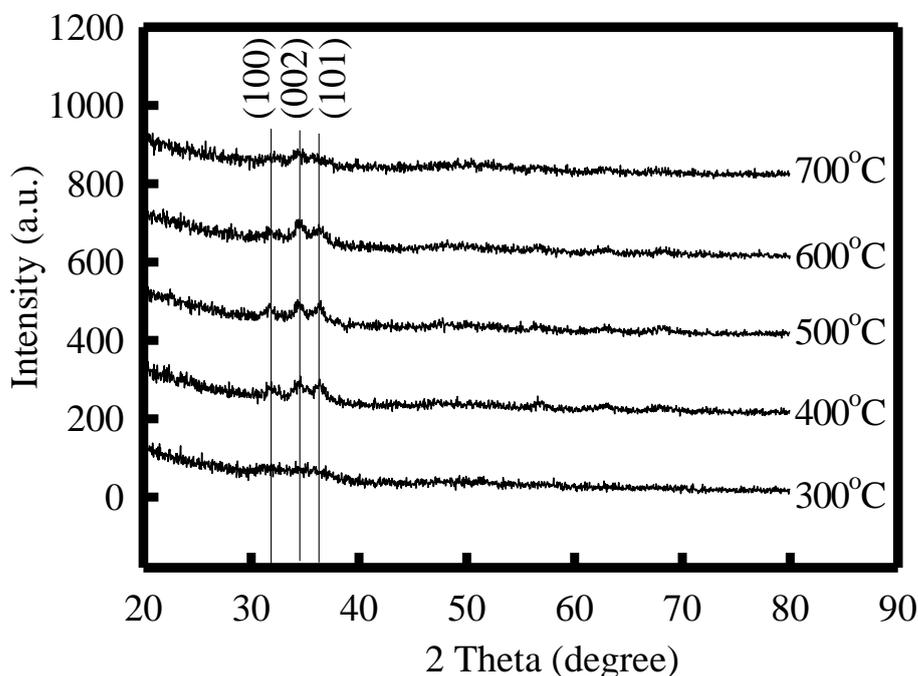


**Figure 5.** XRD patterns from ultra-thin ZnO films treated under different annealing temperatures.

The ZnO films annealed over 400 °C show the preferred (100), (002), and (101) orientation, with the c-axis perpendicular to the substrate surface. Together with the finding in previous section, the primary ZnO crystallites aggregate to larger secondary particles minority during annealing. This crystal state transition during annealing creates some orientations, and contributes into the peaks for XRD spectra. It should be noted that the intensity of the diffraction peaks increases with increasing annealing temperature. This observation is similar to the literature report on diffraction angles [20]. A study from Hsieh et al. mentions that the intensity of peak depends on the thickness of ZnO films [21]. However, we find for ultra-thin ZnO film the intensity of XRD peak can also affected by annealing temperature. This new effect will be further investigated for active channel layer in TFT devices.

### 3.3 Effect of annealing treatments on the ZnO TFT devices

To verify the quality of sol-gel solution-processed ZnO thin film, TFT devices with ZnO thin film as the channel layer under various annealing treatments are fabricated. Fig. 6 shows the characteristics of drain current versus gate voltage ($I_{DS}$-$V_{GS}$) of the ZnO TFTs with different annealing temperatures. The 100 °C annealed sample in Fig. 6a exhibits only background noise, indicating that the too low temperature treatment cannot fabricate suitable semiconducting film for the device. This

phenomenon is attributed to the insufficient removal of solvent from the fabricated ZnO film. The transistor property for annealing at 200 and 500 °C is also observed in Fig. 6a, but the electrical properties of 200 and 250 °C are still challenged and unsatisfactory.  Once the annealing temperature on ZnO ultra-thin film is raised to 300-600 °C, the excellent transistor property for these samples is appeared. This observation means that 300-600 °C treatment can sufficiently remove all unstable molecules in the semiconductor ZnO ultra-thin film and stabilize the film with minor interfacial defects. For example, the excellent device demonstrates desirable high-operating voltage n-type TFT characteristics at an operating voltage of $V_{DS} = 5$ V, and the on/off current ratios can be up to $10^7$ under 500 °C annealing condition.
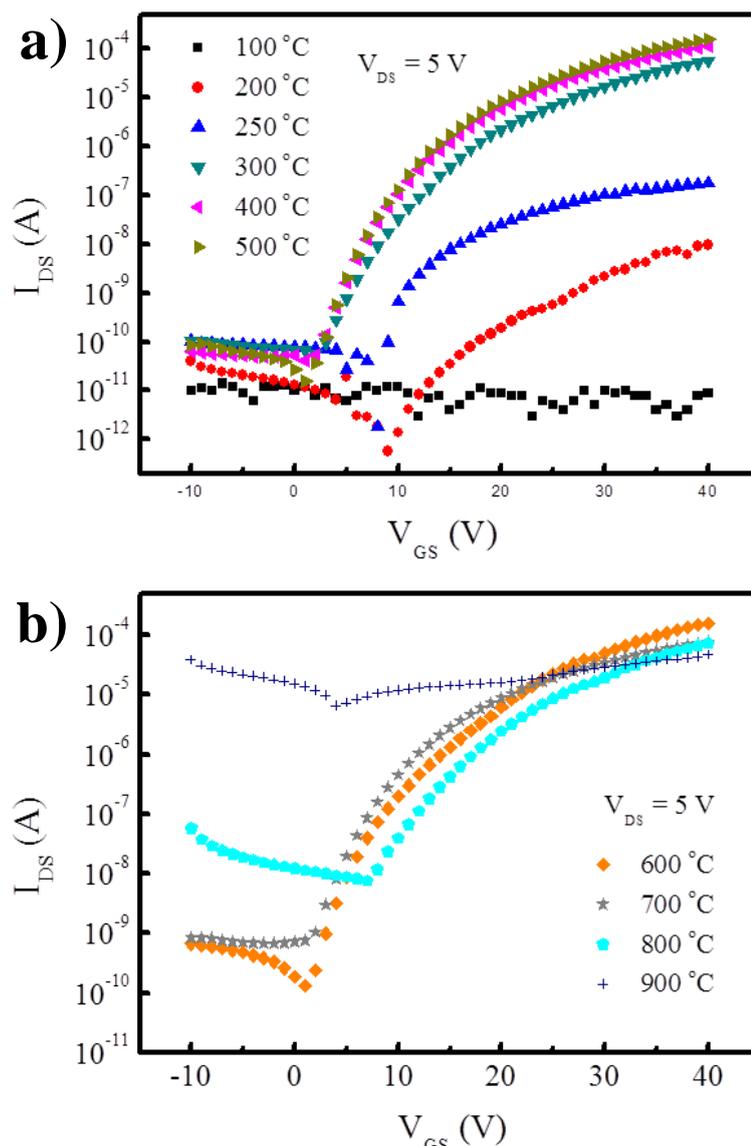


**Figure 6.** Effect of annealing temperatures on transfer characteristics ($I_{DS}$-$V_{GS}$) of ZnO TFTs in ambient environment: a) 100 to 500 °C, and b) 600 to 900 °C.

However, in Fig. 6b when the annealing temperature exceeds 600 °C, the transistor property deteriorates with increasing temperature from 600 to 900 °C. Fig. 6b indicates the electrical property

for device becomes very poor under 800 and 900 °C annealing treatments. To help understanding the performance of TFT of ultra-thin ZnO films with various temperature treatments, the obtained device parameters are summarized in Table 1. The threshold voltage ($V_{th}$) is extracted from $(I_{DS})^{1/2}$ versus $V_{GS}$ plot. The saturation mobility ($\mu_{sat}$) is calculated from the following equation [22]

$$I_{DS} = \frac{\mu_{sat} C_i W}{2L}(V_{GS} - V_{th})^2 \qquad V_{DS} > V_{GS} - V_{th} \qquad (1)$$

Where, $C_i$, W, L, $V_{GS}$, and $V_{th}$ are the capacitance of the gate dielectrics per unit area, the channel width, the channel length, the gate bias, and the threshold voltage, respectively. As shown from Table 1, the electrical performance of the devices is improved upon increasing the annealing temperature from 300 to 500 °C. The respective $\mu_{sat}$ increases from 0.95 to 1.78 cm$^2$ V$^{-1}$ s$^{-1}$, the respective on-current increases from $5.7 \times 10^{-5}$ to $1.6 \times 10^{-4}$ A, the respective threshold voltage from 9.7 to 17.3 V, and the respective on/off current ratio increases from approximately $10^6$ to $10^7$. Although the 500 °C annealed sample exhibits superior performance, sample treated at 300 °C annealing also demonstrates with acceptable electrical properties and is more suitable for low temperature fabrication in the future flexible electronic devices [23]. Hoffman and coworkers [5] has used the very expensive method of ion beam sputtering and rapid thermal annealing (600-800 °C) to fabricated transparent ZnO channel layer TFT where the reported threshold voltage and mobility are 10-20 V and 0.3 to 2.5 cm$^2$ V$^{-1}$ s$^{-1}$. Our low-cost, ultra-thin, transparency and high-quality ZnO TFT from very simple and relatively low-temperature (300-500 °C) of sol-gel processing on the semiconductor layer exhibits the comparable electrical property with the literature method.

In Table 1, variation of annealing temperature significantly influences the charge mobility and on-current of the ZnO TFTs. What is the decisive reason of the annealing-related effect? Literatures has reported that the increase of annealing temperature would allow the ultra-thin ZnO films to create more oxygen vacancies during the annealing process [24,25]. Hence, it could be expected that the formation of the oxygen vacancies involves the electronic carrier generation in the semiconducting ZnO channel.

**Table 1.** Various electrical parameters of ultra-thin ZnO transistors treated with different annealing temperatures from 300 to 700 °C.

| Annealing temperature (°C) | Saturation mobility (cm$^2$ V$^{-1}$ S$^{-1}$) | Threshold voltage (V) | On-current (A) | On/off current ratio |
|---|---|---|---|---|
| 300 | 0.95 | 17.3 | $5.7 \times 10^{-5}$ | $1.1 \times 10^6$ |
| 400 | 1.32 | 15.0 | $1.1 \times 10^{-4}$ | $3.6 \times 10^6$ |
| 500 | 1.78 | 14.5 | $1.6 \times 10^{-4}$ | $2.1 \times 10^7$ |
| 600 | 1.59 | 13.7 | $1.6 \times 10^{-4}$ | $1.2 \times 10^6$ |
| 700 | 0.47 | 9.7 | $7.7 \times 10^{-5}$ | $1.4 \times 10^5$ |
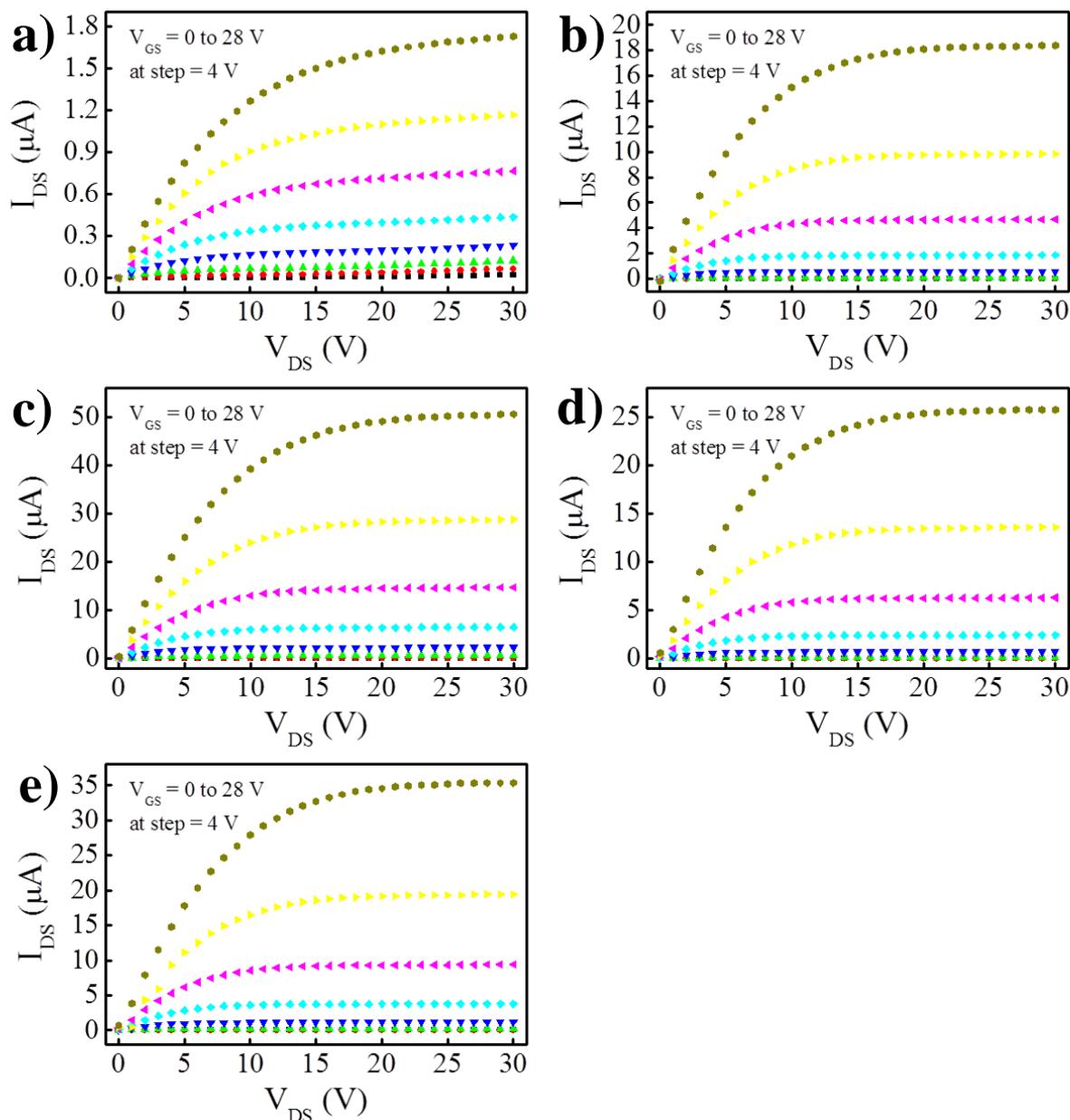
**Figure 7.** Output characteristics ($I_{DS}$-$V_{DS}$) for ultra-thin ZnO transistors in ambient environment treated at a) 300 °C, b) 400 °C, c) 500 °C, d) 600 °C, and e) 700 °C, respectively. Gate bias (positive voltage) is from 0 to 28 V.

The device property in Table 1 demonstrates the trend of on-current and saturation mobility is proportional to the annealing temperature up to 500 °C. Since the conductivity of ZnO film is directly related to the number of electrons which formed by the ionization of the interstitial zinc atom and oxygen vacancies from ZnO crystals. The increase in on-current of ZnO films with the annealing treatment is mainly from the oxygen vacancies. This is because the oxygen vacancies formed by oxygen annihilation in the ZnO crystals from high temperature condition. In addition, when the annealing treatment is performed in a reducing atmosphere or low temperature range, the carrier's concentration may increase by desorption of oxygen in the grain boundaries which previously act as

traps for the carriers [26]. Therefore, the enhancement of the saturation mobility caused by increasing annealing temperature during 300-500 °C can be explained. However, the presence of annealing temperature at high temperature range predominantly functions as the charge oxygen vacancies. The above charge carriers diminish obviously as ZnO thermally treated from 600 °C to 900 °C. The loss of oxygen vacancy upon high temperature treatment observed in Fig. 6b and Table 1 leads to the reduction trend of the saturation mobility and on-current with the temperature.

*3.4 Output characteristics and long-term reliability of the 3.7-nm-thickness ZnO TFT devices*

Fig. 7a-e shows the output characteristic of 3.7-nm-thickness ultra-thin ZnO transistors treated from 300 to 700 °C. Good ohmic contact property at the ZnO interfaces is observed for all samples due to the near same switching on drain current ($I_{DS}$) at 0 V drain voltage ($V_{DS}$). Under various gate voltages, all the drain current sharply increases with drain voltage in 0-5 V, gradually increases with drain voltage in 5-20 V, and saturates with drain voltage in 20-30 V. Upon repeated sweep tests, the ZnO TFTs exhibits consistent performance with a clear linear, curve and saturated behaviors. This observation reflects no degradation of device performance from repeated $I_{DS}$-$V_{DS}$ tests. Moreover, once increasing annealing temperature, the maximal output drain current at 28 V gate voltage is first increased from 300 to 500 °C and then decreased from 500 to 700 °C. This phenomenon has explained in previous section probably due to the number of electrons, oxygen vacancies and carrier scattering effect. Therefore, the annealing temperature strongly affects the output performance of the ZnO TFTs, and the selection of suitable annealing temperature is a very critical parameter for zinc acetate solution-processed ultra-thin film transistors in future industrial application.

Long-term reliability is always a major concern point for solution-processed device due to the effect of residual material after annealing treatment. In order to verify the reliability of our ultra-thin ZnO TFT devices, a long-term duration (in the ambient environment) on output characteristics up to 100 days is carried out in Fig. 8. The photograph in Fig. 8a describes an array of sol-gel solution-processed ultra-thin ZnO TFTs patterned on area of $3 \times 3$ cm$^2$. Fig. 8b-d indicate the retention characteristics of $V_{th}$ shift, on/off current ratio, and $\mu_{sat}$ of the 300 °C (low temperature range) annealed ZnO device, respectively. In comparison with the initial electrical property (i.e. first day: $V_{th}$= 17.3 V, current ratio= $1.1 \times 10^6$, and $\mu_{sat}$= 0.95 cm$^2$ V$^{-1}$ s$^{-1}$), the respective maximal shifts of 100-day duration for $V_{th}$, on/off current ratio, and the $\mu_{sat}$ are near 16, 20, and 14%. This long-term observation for the developed ultra-thin ZnO TFTs indicates the variation of output electrical property can be effectively controlled below 20%. This finding is beneficial for future application of this reliable ZnO TFTs on various fields such as small feature TFT, light emitting diode and flexible panel. In addition, we observe that the trend of $V_{th}$ shift is toward the positive gate voltage regime, and the amount of the $V_{th}$ shift slightly increases as a function of time period. However, the positive value of $V_{th}$ shift is probably caused by the depletion of carriers from the adsorption of oxygen during the room temperature measurements. This result implies that the slight degradation of on/off current ratio and saturation mobility are mainly correlated to the trend of positive shift of $V_{th}$ during the 100-day measurement. Therefore, the long-term reliability of such ZnO TFTs should have a significant dependence on the

amount of adsorbed oxygen during ambient environment. However, this issue is not a problem because common commercial device has been well package to avoid the above damage mechanism.
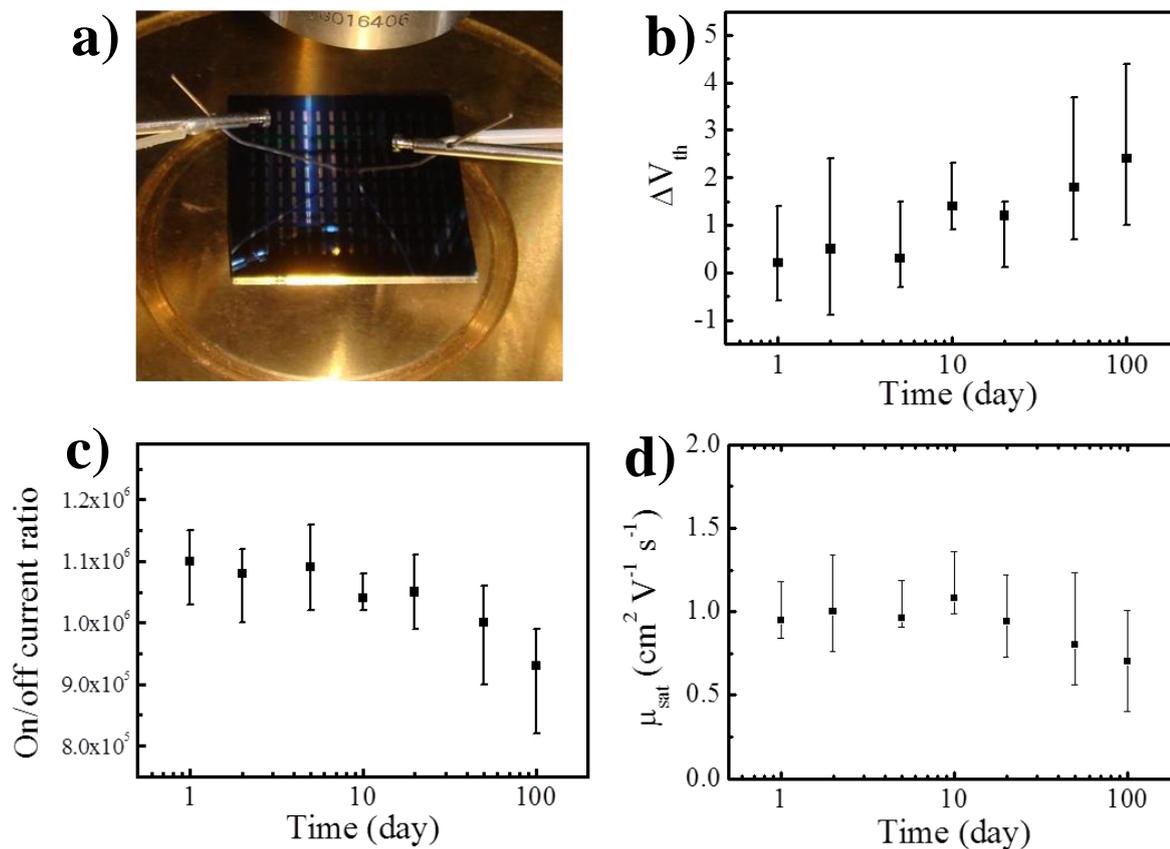


**Figure 8.** Output characteristics and long-term reliability of the 3.7-nm-thickness ZnO TFT devices: a) photograph of an array of ultra-thin ZnO transistors patterned on area of $3 \times 3$ cm$^2$, b) 100-day duration of threshold voltage shift, c) 100-day duration of on/off current ratio, and d) 100-day duration of saturation mobility.

## 4. CONCLUSIONS

We have successfully used sol-gel solution-processed method under electroless condition to fabricate ultra-thin 3.7-nm-thickness ZnO TFT devices on p-type silicon substrate, and these devices have subjected to various temperature treatments ranging from 300 to 700 °C. The TEM, AFM and XRD analyses confirm that the unprecedented sol-gel solution-processed ZnO films could be affected from various annealing treatments, and their plausible application in TFTs from the formation of an ultrathin, conformable, and as a coherent semiconductor layer with amorphous to crystalline-like phase. The surface roughness of ZnO films indicates an increase of the roughness with annealing temperature. Upon 300 to 700 °C film treatment, the transfer characteristics demonstrate the excellent electrical behavior in terms of threshold voltage, saturation mobility and on/off current ratio. Moreover, the long-term reliability after 100-day duration confirms the excellent performance of the ultra-thin ZnO TFT devices with only less than 20% degradation. All above device degradation is caused by the

depletion of carriers from the adsorption of oxygen during the room temperature environment. The spin-coated sol-gel solution process to fabricate TFT devices is a potential and future method for low-temperature and large-area flexible electronic devices and miniaturized bioelectronic sensors.

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