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Charge Storage Characteristics of Pi-Gate Poly-Si Nanowires TaN-Al_2O_3-Si_3N_4-SiO_2-Si Flash Memory

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This work presents a novel TaN-Al_2O_3-Si_3N_4-SiO_2-Silicon (TANOS) nonvolatile memory (NVM) with a structure that comprises Pi-gate (π-gate) nanowires (NWs) structure. The Pi-gate structure in this TANOS NVM increases on current (I_{on}), decreases the threshold voltage (V_{th}) and the subthreshold slope (SS), and enlarges the memory window (ΔV_{th}). Furthermore, the use of high-k Al_2O_3 and a metal gate TaN structure enhances the program/erase efficiency and reliability. This NVM device has a high fast program/erase (P/E) speed; A 3 V memory window can be achieved by applying 18 V for only in 10 μs. With respect to endurance and high-temperature retention characteristics, the 70 % and 60 % of the initial memory window was maintained after 10^4 P/E-cycle stress, and ten years of data storage, respectively. Two-bit operation is achieved and retention characteristics are favorable because of the localized charge trapping in the nitride layer.

Keywords: TaN-Al_2O_3-Si_3N_4-SiO_2-Silicon (TANOS), nonvolatile memory (NVM), nanowire (NW), two-bit, poly-Si

1. INTRODUCTION

Flash memory, a nonvolatile memory, is extensively adopted in portable products owing to its high density and low cost [1]. Recently, efforts have been made aggressively to scale-down flash memory for high density, which follows Moore's law, making device fabrication increasingly difficult. 3D multi-layer-stack memory that is based on the poly-Si thin-film transistor (TFT) has subsequently been introduced as ultra-high-density memory [2], [3]. NVM that is based on the poly-Si TFT has also attracted considerable attention for use in display panels, because of its excellent performance and ease

of integration in active matrix liquid crystal display (AMLCD), ushering in a new era of system on panels (SOP) [4], [5].

Charge trapping polysilicon-oxide-nitride-oxide-Si (SONOS) type flash memory devices has the potential candidate to replace conventional floating-gate NAND Flash devices in the sub-30 nm technology node [6], [7]. SONOS devices have several advantages over the conventional floating gate device, which include fast programming, low-power operation, high-density integration, and good reliability characteristics. According to recent studies of SONOS-type flash, TANOS structure flash memory [8]-[10] exhibits excellent performance because of its immunity to gate injection when metal gate TaN with a high work function is used. A high P/E speed is achieved using the high-k material, Al_2O_3, and good reliability is achieved by exploiting the discrete trapping properties of Si_3N_4. Therefore, TANOS flash memory is a promising future high-density charge trapping layer flash memory.

The unique feature of two-bit per cell operation of SONOS-type flash memory is based on Si_3N_4 localized charge trapping, and the nonconducting property of the charge storage material. This two-bit per cell operation has attracted many attention because it doubles the storage density of flash memory [11], [12].

As has been well established, the multi-gate nanowire channels (NWs) structure can substantially improve the flash memory performance [13]-[15]. Therefore, TANOS NVM and the Pi-gate NWs structure are combined herein to achieve a high P/E speed, good reliability and two-bit per cell operation for 3D high-density NVM and SOP applications.

2. EXPERIMENTAL DETAILS

These devices were fabricated by initially growing a 400 nm thick silicon dioxide layer on 6 inch silicon wafers. A 50 nm thick undoped amorphous-Si layer was deposited by low-pressure chemical-vapor deposition (LPCVD) at 550^{o}C and this thin layer was following solid-phase crystallized (SPC) at 600^{o}C for 24 hours in nitrogen ambient. The patterns of the active layer were defined by electron beam (e-beam) direct writing. The active layer was defined as ten strips of multiple 86 nm NWs. Numerous NWs are for high drain current purpose. The photoresist patterns were transferred by reactive ion etching (RIE) using Cl_2/Ar mixed etchant gas. A 10 nm thick thermal SiO_2 layer was grown as the tunneling oxide. Above the thermal SiO_2, an 7 nm thick Si_3N_4 was deposited by low-pressure chemical vapor deposition (LPCVD) as the electron trapping layer and a 10 nm thick Al_2O_3 was deposited by metal-organic chemical vapor deposition (MOCVD) as the blocking oxide. Two layers, 30 nm thick TaN and 80 nm thick poly-Si were deposited as the control gate and transferred by e-beam direct writing and RIE. Then, the self-aligned source, drain, and gate regions were implanted with phosphorous ions at a dose of 5×10^{15} cm^{-2} and activated by rapid thermal annealing at 900^{o}C for 40 s in nitrogen ambient. The work function value of TaN metal after annealing is about 4.7 eV [16]. The 200 nm thick tetra-ethyl-ortho-silicate (TEOS) oxide and 300 nm thick Al-Si-Cu were deposited as a passivation layer and metallization layer, respectively. Finally, the devices

were then sintered at 400 °C in hydrogen ambient for 30 minutes. The single-channel (SC) structure (W = 1 μm) NVM with a conventional top-gate was also fabricated for comparison.

3. RESULTS AND DISCUSSION

Figure 1(a) presents the top view of a Pi-gate NWs TANOS Memory. Figure 1(b) shows the device's cross-section plot along the AA' direction. Figure 2(a) shows the transmission electron microscopic (TEM) photograph along the BB' direction of figure 1(a). Figure 2(b) shows the enlarged image of figure 2(a). It clearly shows the Pi-shaped gate structure on NW, and the four corners of the NWs are surrounded by the control gate. The physical width of each NW of the ten channels is 86 nm. Three layers 10/7/10 nm of $SiO_2/Si_3N_4/Al_2O_3$ are stacked as the gate dielectric.

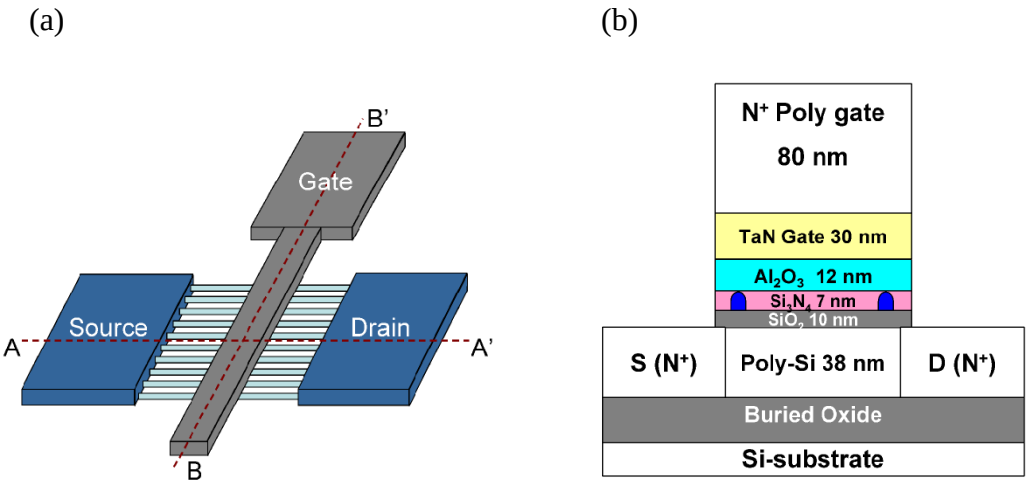

Figure 1. (a) Top view scheme of the Pi-gate NWs TANOS NVM. (b) Cross-section scheme of TANOS device along A-A' direction.

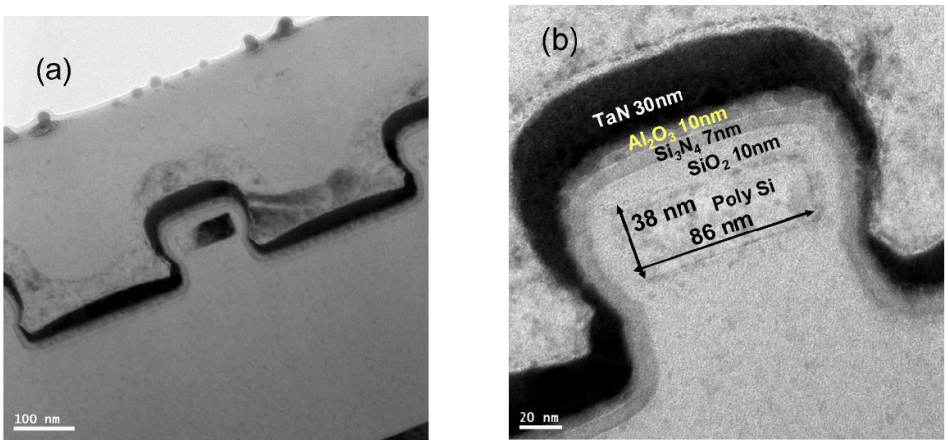

Figure 2. (a) TEM image of Pi-gate NWs TANOS NVM structure. (b) Magnification TEM image of figure 2(a). The stacked gate dielectric are SiO_2 =10 nm / Si_3N_4 = 7 nm / Al_2O_3 = 12 nm, and each poly-Si NW width is 86 nm.

Figure 3 plots the I_{ds}-V_{gs} curve of the poly-Si NWs and the single-channel (SC) TANOS memories. The devices are programmed by Fowler-Nordheim (FN) tunneling at a gate bias of 18 V for 1 μs. The drain voltage (V_{ds}) of the I_{ds}-V_{gs} curve is 0.5 V and V_{gs} is swept -1 V to 8 V. The memory window (ΔV_{th}) is 2.8 V of the NWs devices, which is larger than that of the SC TANOS device. The subthreshold slope [$SS = d V_{gs} / d \log (I_{ds})$] is a parameter to describe the gate control toward channel conductance. The SS are 0.35 V/dec and 0.46 V/dec for the NWs and the SC fresh cells, respectively. Because of the high electrical field near the NWs corners of the Pi-gate structure, the Pi-gate NWs device has better gate control than the SC device.

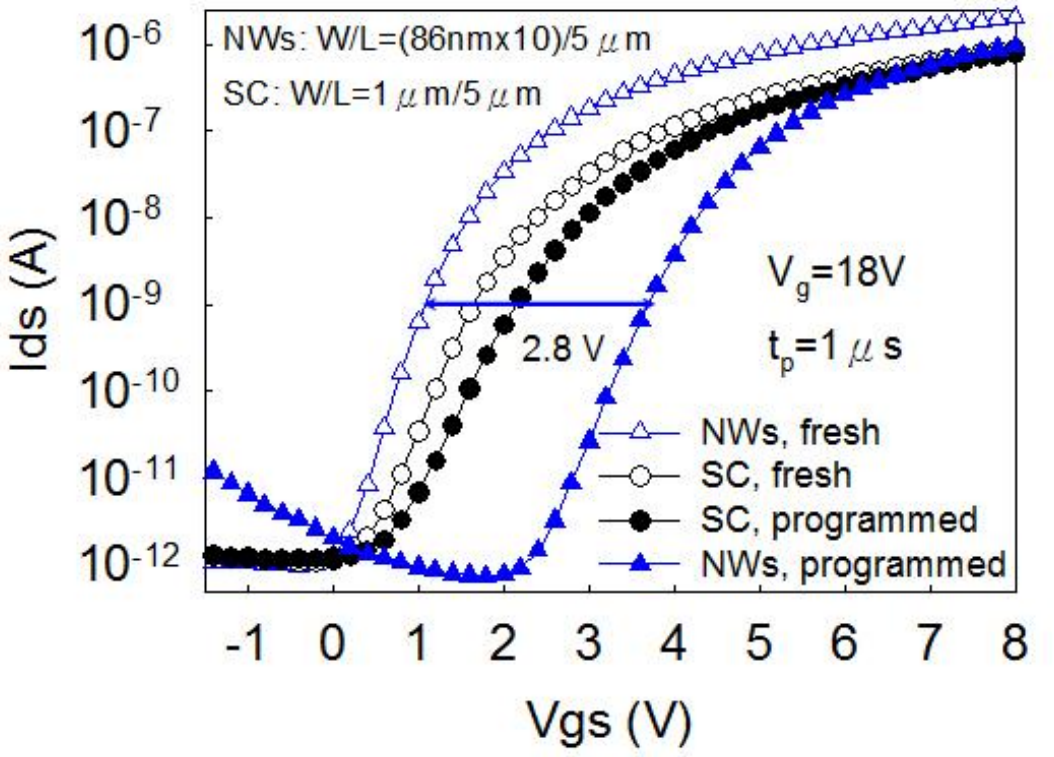

Figure 3. I_{ds}-V_{gs} curve of the poly-Si NWs and the single-channel (SC) TANOS memories.

Fig. 4 plots the program and erase (P/E) characteristics of the NWs TANOS devices. The P/E operations proceed by the FN tunneling at V_{gs} = 12, 15, 18 V and V_{gs} = -15, -18, -21 V with $V_d = V_s$ = 0 V, respectively. ΔV_{th} increases with the P/E pulse width and the bias. The ΔV_{th} of the NWs devices can exceed 3.0 V in only 10 μs at V_{gs} = 18 V. This efficient program result reveals that the high-k Al_2O_3 increases the gate coupling ratio and the Pi-gate structure enhances the electric field in the tunneling oxide at the corners of the NWs. With respect to the erase characteristics, ΔV_{th} is directly proportional to the erase bias and time. No erase saturation effect occurs even at high erase bias or over a long erase time. This result is explained by the high work function of the TaN, 4.7 eV, which prevents the injection of electrons from the gate [8].

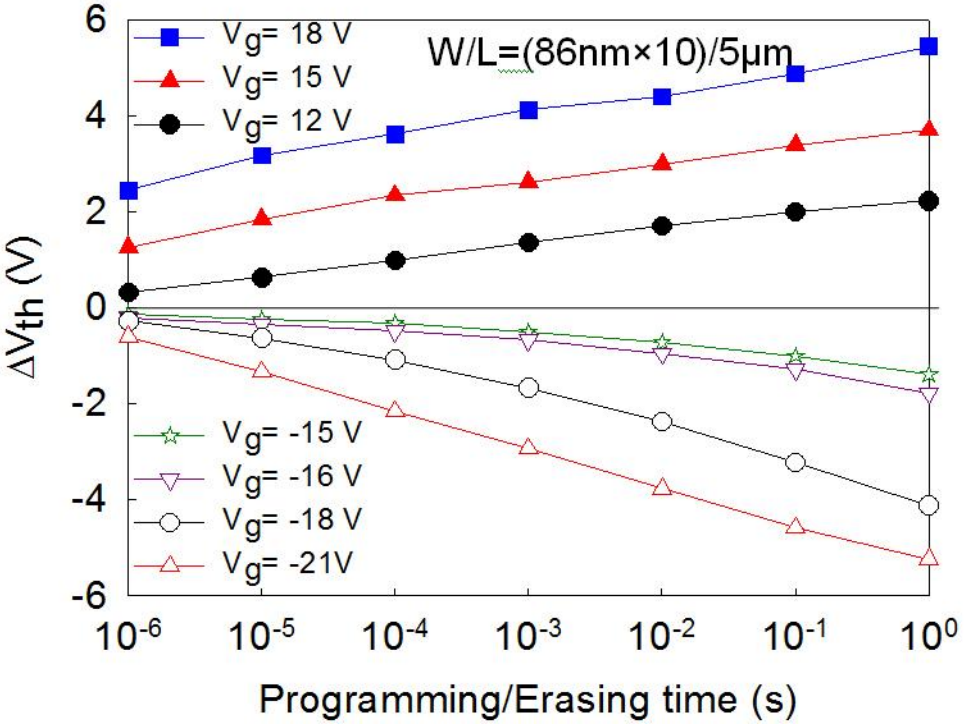

Figure 4. Program and erase (P/E) characteristics of the NWs TANOS devices.

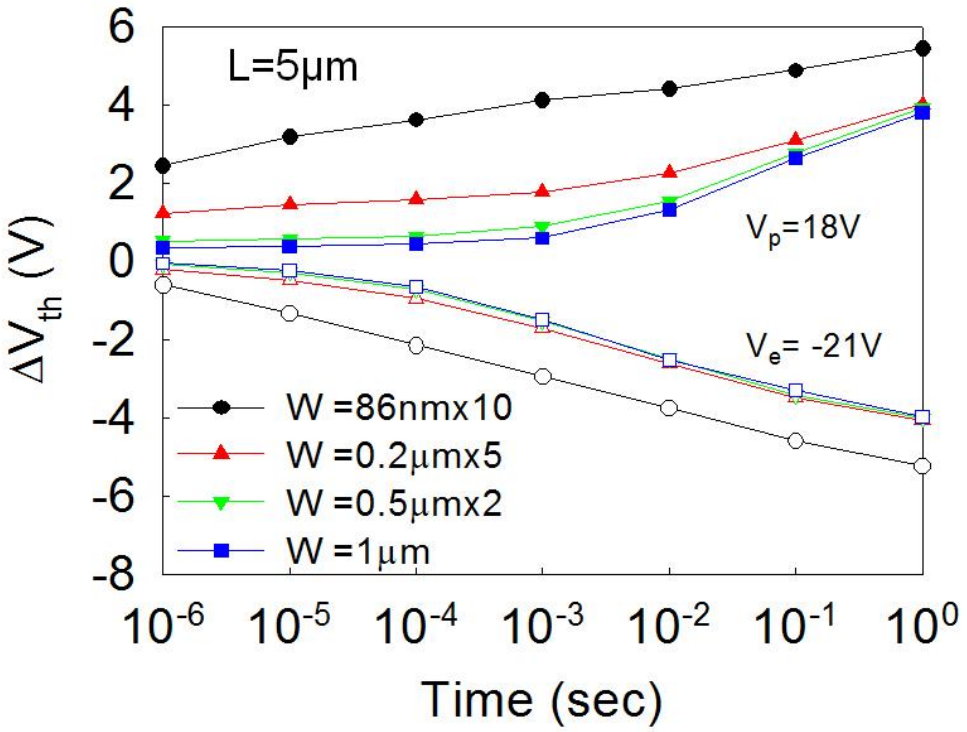

Figure 5. Program and erase characteristics of various different channel width and length TANOS devices

Figure 5 plots P/E speed obtained with various channel widths and numbers of TANOS NVM for a fixed P/E bias of 18 / -21 V. The P/E speed increases as the width of each channel decreases. The ten-NW device performs the fastest P/E speed because it forms a Pi-gate structure (Figure 2b).

Figure 6 plots the endurance characteristic of the Pi-gate NWs TANOS NVM. Two erasing conditions, V_{gs} = -24 V with erasing time (t_e) = 2 ms and V_{gs} = -25.5 V with t_e = 0.2 ms, were applied in the endurance study. Applied the erase pulse with lower voltage but longer pulse width, the NVM device performs better endurance. 70 % of its initial memory window was maintained after the NVM device suffered 10^4 P/E cycles. This result is explained by the fact that the degradation of the tunnel oxide (SiO_2) in TANOS NVM mainly depends mainly on electric filed. Additionally, the endurance curves rise slightly as the number of P/E cycles increases because some of the electrons are trapped in the deep state of Si_3N_4, making erasure difficult.

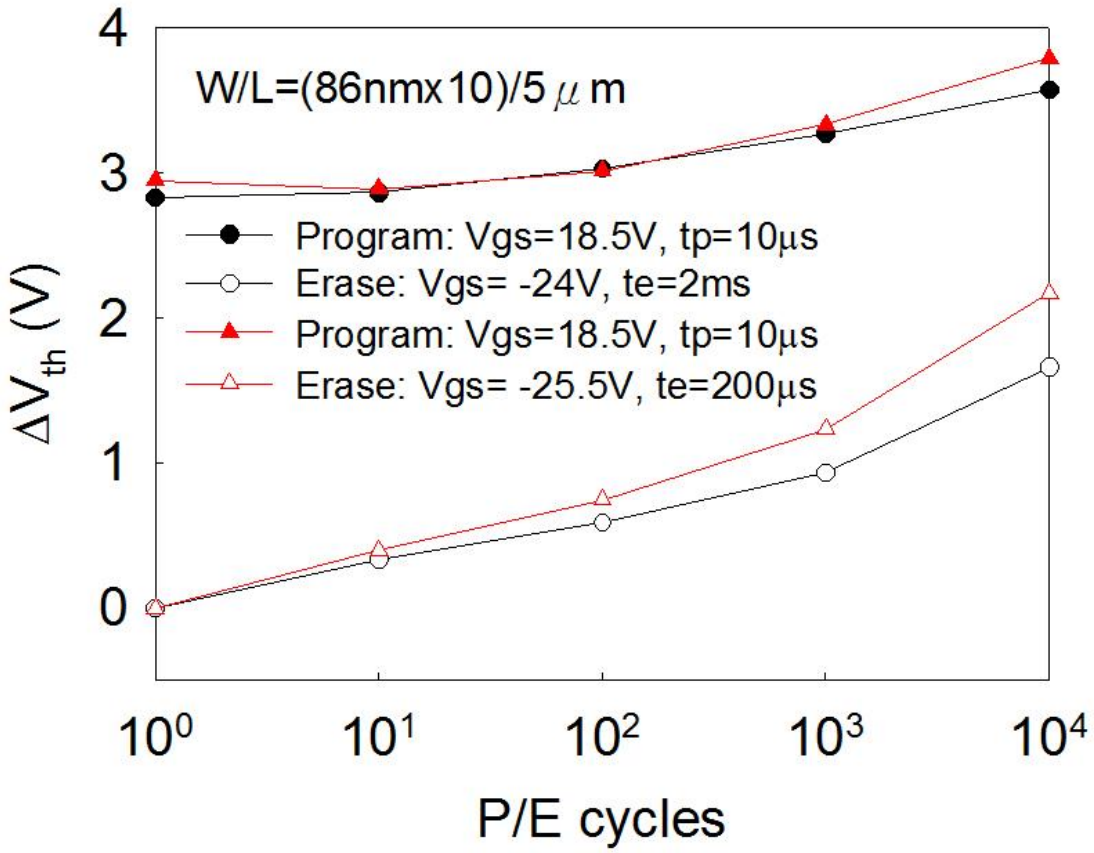

Figure 6. Endurance characteristics of Pi-gate NWs TANOS NVM.

Figure 7 plots the high temperature (85 ^oC) retention of the fresh Pi-gate NWs TANOS NVM cell and that after 10^4 cycles, respectively. The maintained memory window of the fresh cell was predicted to be 60 % of the initial window, and that of the 10^4 P/E cycle-stressed device was predicted to be 40 % of memory window after ten years. Charge may be loss through the Al_2O_3 blocking layer, which was thin in this study, with a thickness of only 10 nm. The retention was further improved by using a thick Al_2O_3 blocking layer or adding a sealing oxide between the Al_2O_3 and Si_3N_4 layers [17].

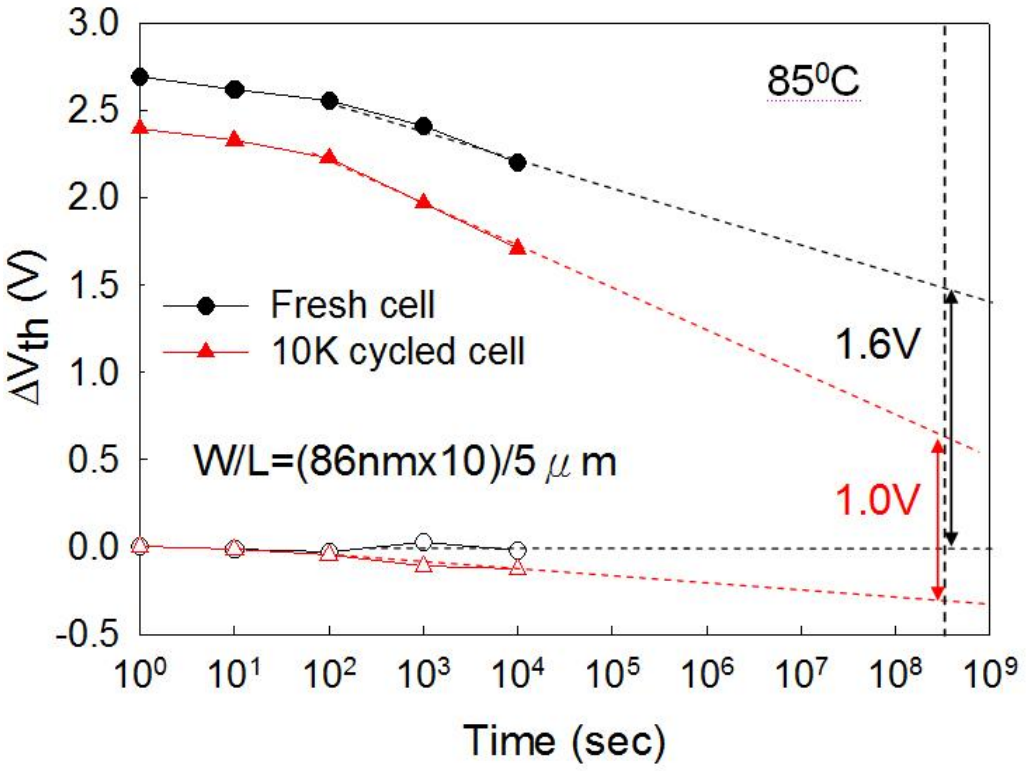

Figure 7. Retention characteristics of Pi-gate NWs TANOS NVM.

A flash memory device can be programmed by channel hot electron (CHE) injection. As is generally accepted, the programming speed that by CHE injection substantially exceeds that by FN tunneling. Figure 8 plots the Pi-gate NWs TANOS NVM threshold voltage shift (ΔV_{th}) versus different gate length (L). The devices were programmed CHE injection with V_{gs} = 10.5 V and V_{ds} = 14 V and a programming time (t_p) of 1s. To become the hot, electrons must gain sufficient kinetic energy from the lateral field in the channel to surmount the Si/SiO_2 barrier [18]. Experimental results indicate that ΔV_{th} declines as L increases. For devices whose gate length (L) exceeds 2 μm, the ΔV_{th} is close to zero, since none of the electrons is injected into the Si_3N_4 layer. This result is explained by the fact that the lateral electric field in long channel devices is too weak to accelerate electrons as hot electrons. Moreover, poly-Si grain boundaries function barrier to hot electrons and the mean free path of accelerated electrons is limited by the poly-Si grain length (approximately 30 nm by SPC). Therefore, transported electrons may be scattered every 30 nm. However, for a device with a short channel, L = 0.7 μm, the lateral electric field is strong, and can make the electrons hot. These hot electrons overcome the poly-Si grain boundary barrier and become trapped in the Si_3N_4 layer. The ΔV_{th} of the L = 0.7 um device is significant, with a value of 1.5 V. Therefore, the 2-bit operation, preformed by source and drain two-side interchange by CHE injection, could be implemented at device with L of 0.7 μm in this study, but not in devices with an L of over 0.7 μm.

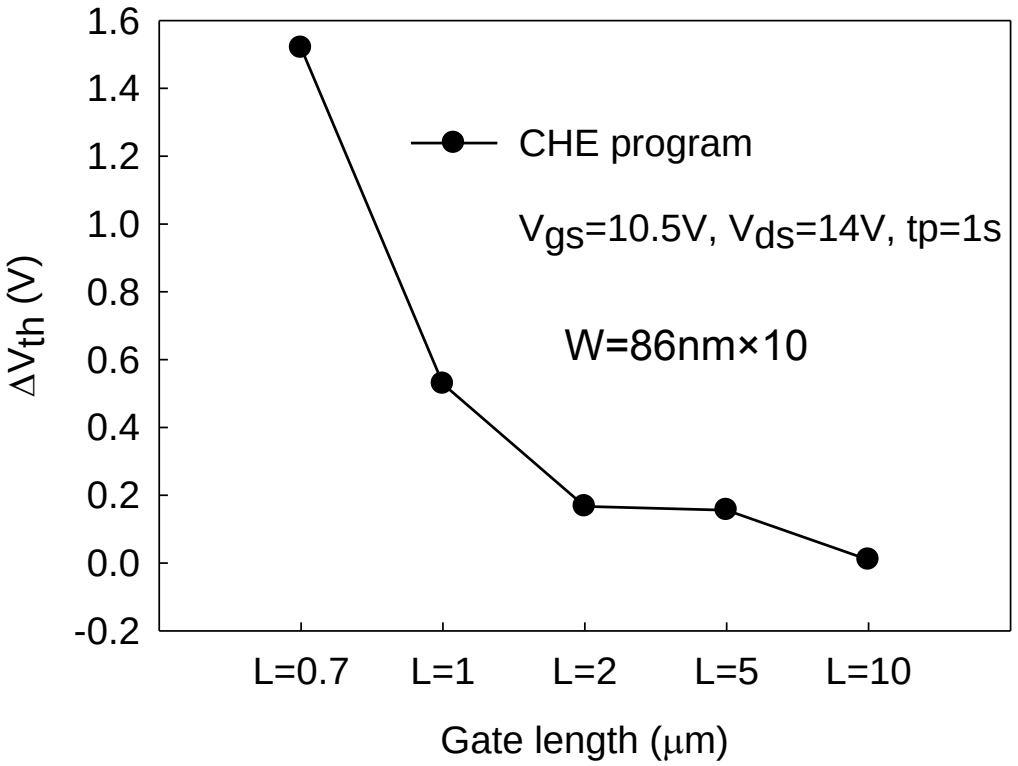

Figure 8. Threshold voltage shift (ΔV_{th}) of the Pi-gate NWs TANOS NVM for different gate length (L).

The two-bit per cell operation is based on localized charge trapping in Si_3N_4, and the non-conducting property of the charge storage material. Figure 9 plots the I_{ds}-V_{gs} curves of the Pi-gate NWs TANOS NVM with two-bit characteristics under CHE injection programming and band-to-band tunneling induced hot holes (BBHH) injection erasing. Table I presents the bias conditions of Pi-gate NWs TANOS NVM under program, erase, and read conditions. In Fig. 9, the logical "1" indicates that electrons were programmed in the storage node. As an example, (Bit-S, Bit-D)-read mode = (0,1)-R means that Bit-S is in its erased state and Bit-D is in its programmed state under reverse reading. To demonstrate the two-bit effect, a programming bias is firstly applied to write electrons into bit-D by CHE injection. The accelerated electrons are injected into the narrow region in nitride layer near the drain junction (inset). Then, V_{read} (V_s) = 4.8 V was applied for reverse reading of and V_{gs} was swept, to yield the (0,1)-R curve. Second, V_{read} (V_d) = 4.8 V was applied for forward reading to yield the (0,1)-F curve. In forward reading, the read voltage had be large enough to generate a depletion region, which can be extended to screen out the localized trapped charges at drain side, such that the programmed cell has low V_{th} (or high current). Thus, a significant threshold shift of ΔV_{th} = 1.5 V between these (0,1)-R and (0,1)-F curves is observed. The second bit (bit-S) is programmed and read by switching the roles of the two junctions, as revealed by the (1,0)-F and (1,0)-R curves.

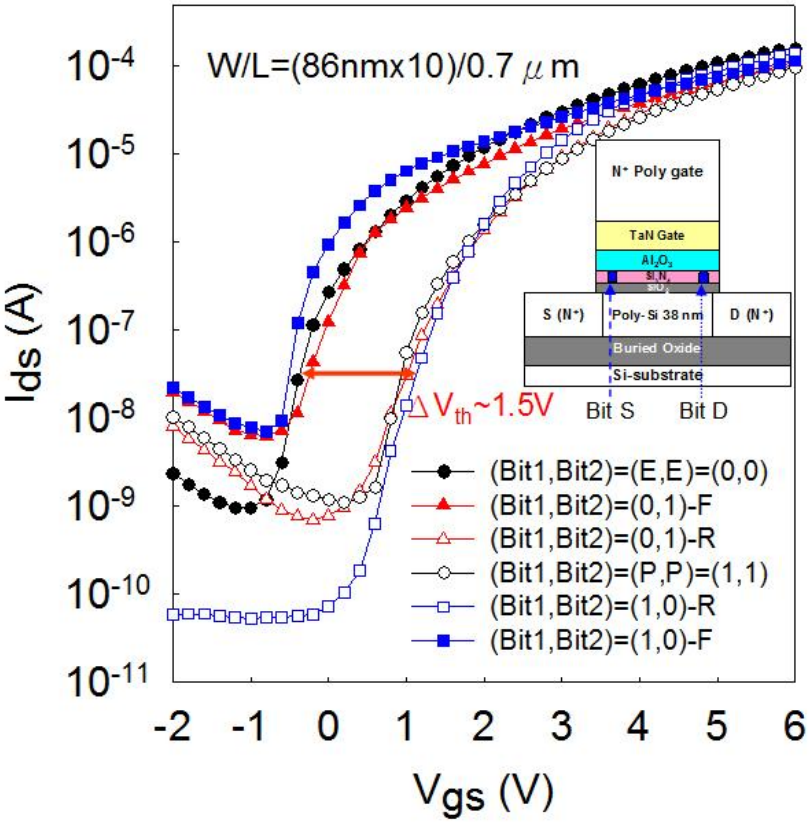

Figure 9. The two-bit I_d - V_g curves of Pi-gate NWs TANOS NVM. As an example (Bit-S, Bit-D)-read mode = (0,1)-R denotes Bit-S in its erased state and Bit-D is programmed under reverse read. High V_{th} is obtained under R-read.

Table I. Operation mechanism and bias conditions utilized Pi-gate poly-Si NWs TANOS NVM with W / L = 86 nm × 10 / 0.7 μm.

	Bit D			Bit S		
	Vgs	Vd	Vs	Vgs	Vd	Vs
Program (V)	10.5	14	0	10.5	0	14
Erase (V)	-10.5	10.5	0	-10.5	0	10.5
Read (V)	0.3	0	4.8	0.3	4.8	0

Figure 10 shows the room-temperature bit-D retention of the of Pi-gate NWs TANOS NVM. To maintain the two-bit capability, the memory window is smaller than that associated with conventional operation (Fig. 7). The ΔV_{th} of the bit-D was predicted to be 66 % of the initial window after ten years. The degradation of retention may arise from charge loss through the Al_2O_3 blocking layer because of the thin Al_2O_3 or the lateral migration of charge in the Si_3N_4 layer.

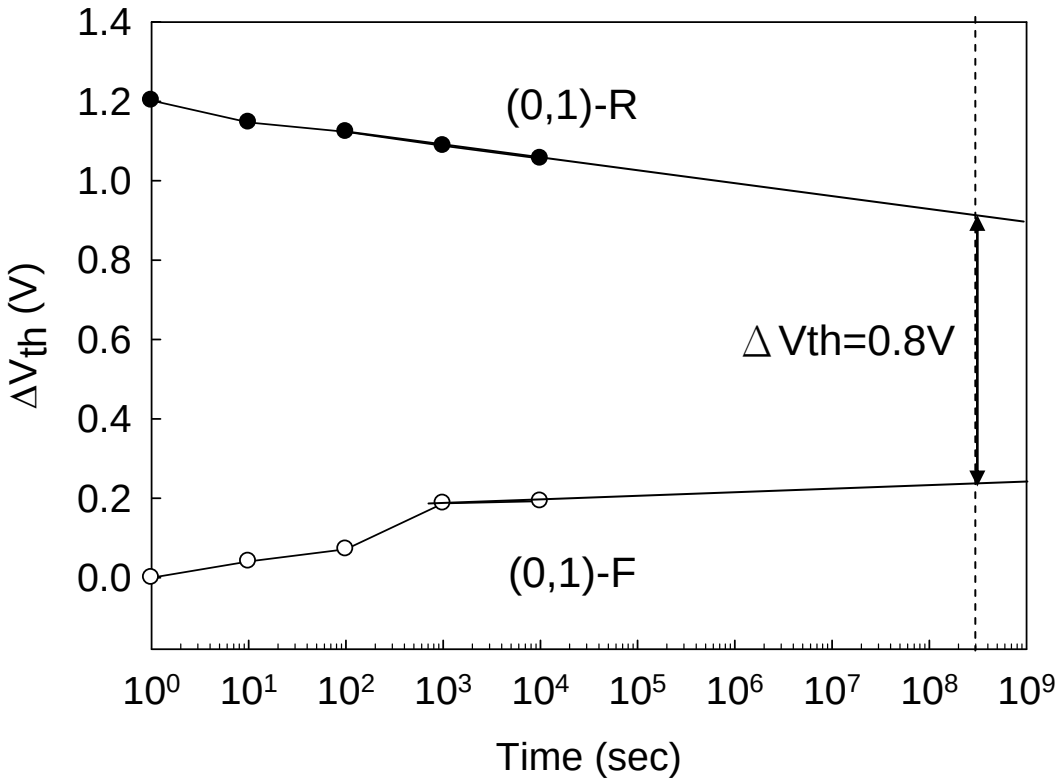

Figure 10. Bit-D retention characteristics of Pi-gate NWs TANOS NVM.

4. CONCLUSIONS

A Pi-gate poly-Si NWs TANOS NVM with high P/E speed and good reliability is demonstrated. A 3 V memory window was achieved by applying 18 V in only 10 μs, because of the high-k blocking layer Al_2O_3 and Pi-gate NWs structure. The use of TaN with a high work function makes this NVM device immune to erasing saturation. With respect to endurance, the 2 V of memory window is maintained after 10^4 P/E stress cycles. With respect to retention, 60% of the initial memory window is maintained after ten years. This retention can be improved by using a thick Al_2O_3 blocking layer or adding a sealing oxide. The two-bit operation capability and its retention also perform of this TANOS device. This investigation examined the feasibility of using a Pi-gate poly-Si NWs TANOS NVM in future 3-D layer-to-layer stacked high-density flash memory and active matrix liquid crystal display system-on-panel (SOP) applications.

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