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Investigation of the Sol-Gel Method on the Flexible ZnO Device

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This paper proposes a sol-gel deposition method applied to ZnO thin film as a semiconductor layer for transistors (TFT). First, various annealing temperatures were applied onto zinc oxide (ZnO) TFT with a bottom gate structure to examine the transistor's characteristics. In annealing at 300 °C, the oxygen vacancies of ZnO thin films demonstrated that the transistor showed the property with an on/off current ratio of up to 10^5 and a μsat of 0.06 cm^2/V-s. Finally, the silicon wafer was substituted by a polyimide substrate, and the sol-gel method in the low-temperature (300 °C) process was developed to fabricate flexible ZnO transistors. The flexible ZnO transistors exhibited a high on/off current ratio (Ion/off) up to 10^7 and a μsat of 0.98 cm^2/V-s.

Keywords: Flexible ZnO Device, Low-Temperature Process, Sol-Gel Method

1. INTRODUCTION

Studies in novel flexible electronics for developing lightweight, low cost, portable, and shock-resistant devices such as displays, solar cells, sensors, and radio frequency identification (RFID) mechanisms have increased considerably [1, 2]. However, a-Si:H and polysilicon, which have been commonly used as channel layers for transistors, have several limitations including high temperatures, photosensitivity, and high cost because of their conventional CMOS processes. In flexible electronics, organic semiconductor thin-film transistors have been researched substantially [3]. Organic transistors can be fabricated by processing at near room temperature, and furthermore, can be compatible with flexible plastic substrates. Despite successful demonstrations with flexible organic TFTs, however, they are generally sensitive to operating conditions, and are also unstable under long-term operation [4].

Generally, metal oxide thin films used as electrodes in flat panel displays include In_2O_3, SnO_2, and ZnO. Indium is currently the most commonly used material, but is toxic it is not as cost-effective as zinc. In recent years, ZnO thin films have been considered good candidates for use as metal oxide materials because of their high visible transmittance, conductivity, and low-cost fabrication [5].

Formations of ZnO TFT can be achieved using many methods, including pulsed laser deposition (PLD), metalorganic chemical vapor deposition (MOCVD), and molecular beam epitaxy (MBE). However, these methods are incompatible with flexible electronics manufacturing because either a high-vacuum system or a high-process temperature is required to obtain good electric properties [6].

Currently, most ZnO thin films are deposited by using chemical vapor deposition (CVD) and physical vapor deposition (PVD) methods. CVD and PVD often require a high-vacuum and high-temperature environment, and thus, do not work for flexible electronic roll-to-roll processes integrated for ZnO thin-film deposition. In contrast, the sol-gel method of channel layers offers advantages in enabling the fabrication of a flexible transistor including low cost, low temperature, easy control of deposition parameters, compatibility with large area depositions, and an ability to operate at atmospheric pressure [7, 8, 9, 10, 11].

This paper uses ZnO thin film applied in the channel layer of the transistor to replace OTFT, and the inexpensive and simple solution to deposit the thin film of a channel layer by spin coating. The ZnO TFTs were annealed at low temperature, controlled at approximately 300 °C, and subsequently, polyimide was used to replace the silicon substrate to complete the flexible ZnO TFT.

2. EXPERIMENTAL DETAILS

This study examines the electrical performance of ZnO-based TFTs on various substrates at 300 °C (Fig. 1) with a device structure channel width (W) and length (L) of 2000 μm and 70 μm, respectively. The ZnO precursor solutions were synthesized using zinc acetate dehydrate. These solutions, 0.05M in metal precursors, were prepared in ethanol. These metal oxide solutions were stirred for 30 min at 80 °C before spin coating.

1) Silicon: First, a p-type silicon wafer was treated using RCA clean, and then thermal oxidation was used to grow a SiO_2 film with a thickness of approximately 100 nm. After SiO_2 formation, the surface was treated by oxygen plasma for 30 s. ZrO_2 films were deposited by spin coating at 1000 rpm for 30 s under an ambient temperature of 25 °C. After spinning the ZnO solution, the film was annealed at 300 °C for 1 h in air. Finally, by a thermal evaporation (pressure 10^{-6} Torr) process, the wafer back-plated with Al = 300 nm was defined as the gate electrode; a shadow mask was used to define the source and drain, both plated with Al = 300 nm.

2) Polyimide: All the prepared polyimide was treated with ultra sonication in acetone before deposition of the gate electrode to ensure a clean surface. For preparation of a ZnO-based TFT, a Ti/Au/Ti (7 nm/20 nm/7 nm) film was deposited on the polyimide substrate as a gate electrode. A 250-nm-thick SiO_x layer was grown by plasma-enhanced chemical vapor deposition for the gate insulator. After SiO_x was treated with O_2 plasma to break the chains on its surface, polar and hydrophilic

functional groups such as OH were introduced on the surface, resulting in an increase of surface energy [6]. Because of the increased surface energy of the SiO_x insulation, the coverage of the ZnO thin films on the SiO_x surface was improved. The ZnO precursor solution was spin-coated at 1000 rpm for 30 s onto the SiO_x. The thin films were then annealed at 300 °C for 1 h in air under standard atmospheric pressure. To fabricate the TFT with contact electrodes, a Ti/Au drain and source electrodes with a thickness of 7 nm/20 nm were deposited by vacuum evaporation (pressure of approximately 10^{-6} Torr) through a shadow mask. An electrical measurement of the ZnO devices was performed with an Agilent 4156 probe station.

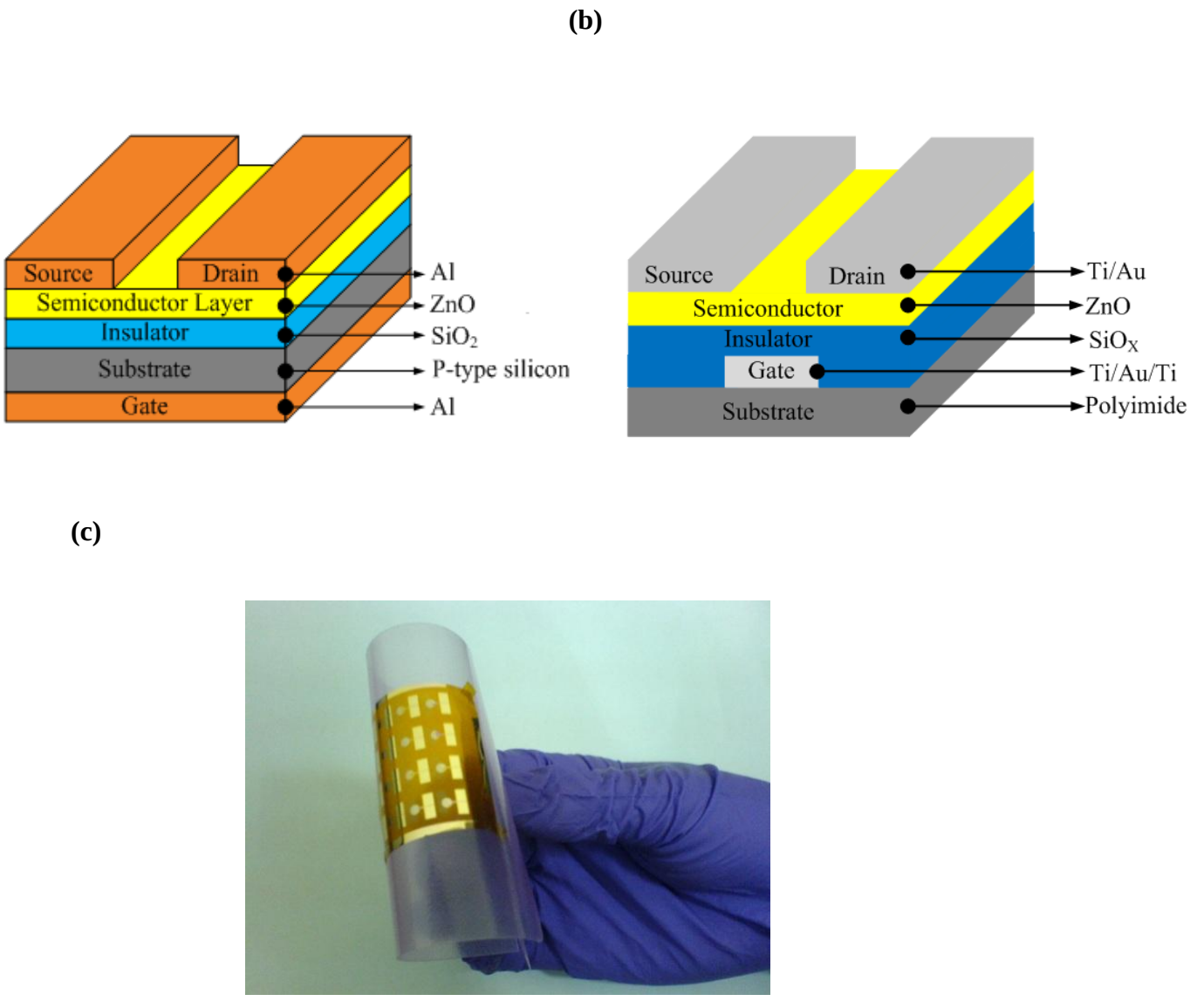
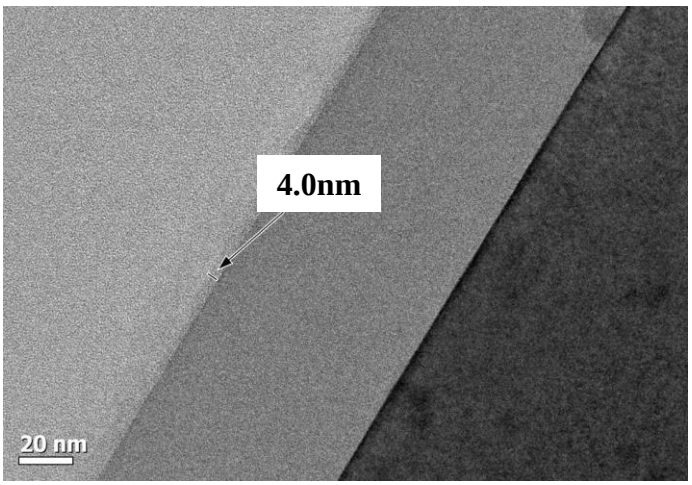


Figure 1. A schematic cross-sectional view of the ZnO structure. (b) Schematic bottom gate structure of a flexible ZnO TFT. (c) Photograph of the flexible ZnO TFT.

3. RESULTS AND DISCUSSION

Fig. 2(a) shows the cross-sectional TEM images of the ZnO/SiO_2 structures annealed at 300 °C. The TEM images show that the sol-gel method deposited a smooth semiconductor ZnO film of approximately 4.0 nm in thickness. The surface morphology of the thin film is important in the transistor. Fig. 2(b) shows the AFM images of the sol-gel-derived ZnO thin films. The root mean square (RMS) roughness of the ZnO thin films was 0.635 nm. For the ZnO thin film annealed at 300 °C, the thin-film surface created by the sol-gel method is still smooth. An electron spectroscopy for chemical analysis (ESCA) of ZnO thin films was performed to investigate the chemical bonding states and the impurity content of the constituent elements at 300 °C.

(a)



(b)

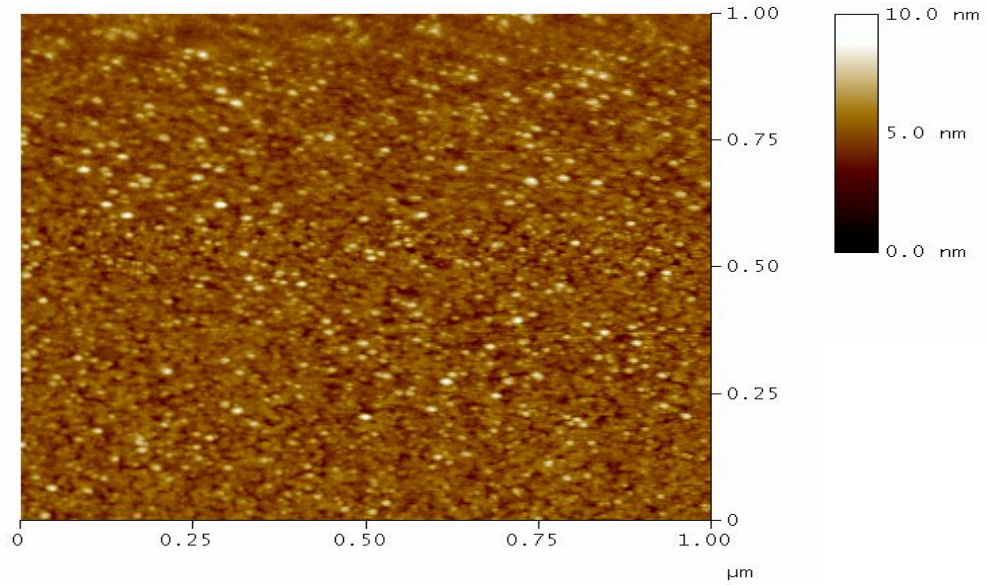


Figure 2. (a) Cross-sectional TEM images of sol-gel-derived ZnO/SiO_2 structures annealed at 300℃. (b) AFM images of the ZnO thin films annealed at 300℃, the scanning area of 1 μm^2

Fig. 3(a) shows the $Zn2p_{3/2}$ spectra of the ZnO thin films annealed at 300 °C. The binding energy of $Zn2p_{3/2}$ from the hexagonal wurtzite ZnO phase was reported at 1022.4 eV [12, 13]. The data in this study were fitted by a Gaussian curve with peaks centered at 1022.25. Fig. 3(b) shows the O_{1s} spectra of the ZnO thin films annealed at different temperatures. The ZnO film's O_{1s} ESCA peak in Fig. 3 can be deconvoluted into a spectra of the three peaks located at 532.9 eV, 531.7 eV, and 530.9 eV. The 532.9 eV peak is assigned to hydroxide, the 531.7 eV peak to oxide lattices with oxygen vacancies (oxygen-deficient), and the 530.9 eV peak to oxide lattices without oxygen vacancies (ZnO). The O_{1s} peak-fitted binding energy peaks are similar to the results of Lim et al. and Kim et al. [14, 15]. Table 1 shows the performance of the ZnO-based TFT and the flexible ZnO TFT. The threshold voltage (Vth) was extracted from $(IDS)_{1/2}$ versus a VGS plot. The saturation mobility (μsat) was calculated from the following equation:

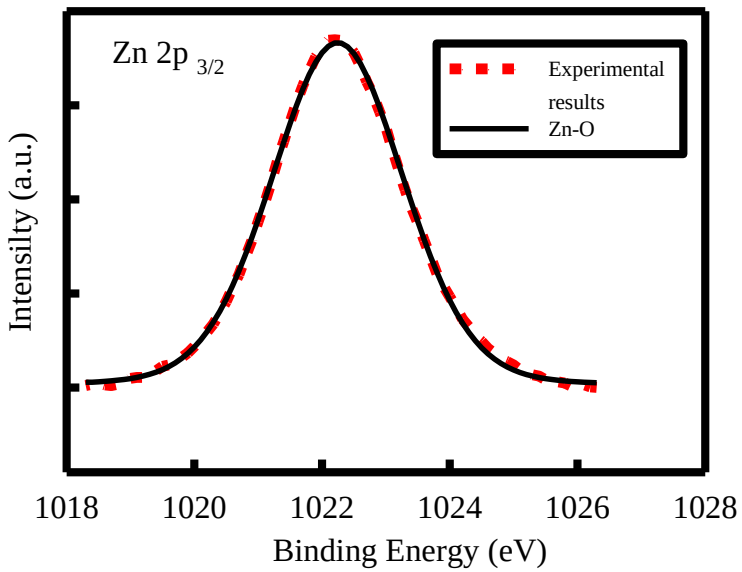
$$I_{DS} = \frac{\mu_{sat} C_i W}{2L}(V_{GS} - V_{th})^2 \qquad V_{DS} > V_{GS} - V_{th}$$

where Ci, W, L, VGS, and Vth are the capacitance of the gate dielectrics per unit area, the channel width, the channel length, the gate bias, and the threshold voltage, respectively.

Table 1. Electrical parameters of ZnO-based TFT and flexible ZnO TFT treated with annealing at 300 °C.

	I_{ON} (A)	I_{OFF} (A)	$I_{ON/OFF}$	V_{TH} (V)	M_{FE} (CM^2/V-S)
ZNO	3.81×10^{-6}	2.18×10^{-11}	10^5	15.6	0.06
FLEXIBLE ZNO	1.15×10^{-4}	9.25×10^{-11}	10^7	12.3	0.98

(a)



(b)

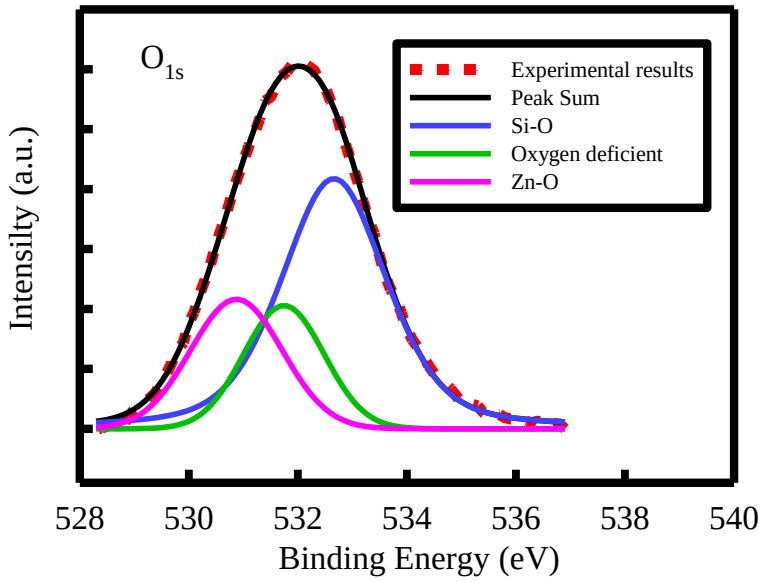
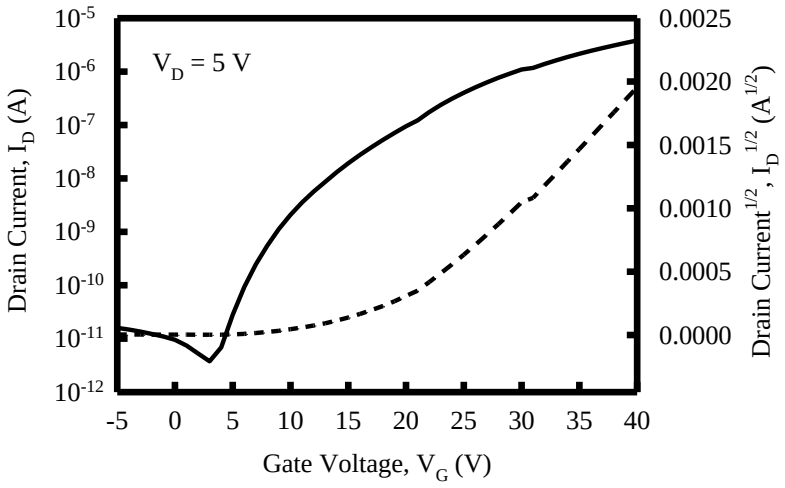


Figure 3.(a) ESCA spectra for the Zn $2p_{3/2}$ signals of ZnO thin film annealed at 300℃. (b) ESCA spectra for the O_{1s} signals of ZnO thin film annealed at 300℃.

Fig. 4(a) shows the drain current-gate voltage (ID-VG) transfer characteristic curves of ZnO TFT annealed at 300 °C with channel lengths of 70 um and widths of 2000 μm. The ZnO TFT exhibited an on-off current ratio (Ion/off) up to nearly 10^5. The on current (Ion) is able to sustain levels as high as 3.81×10^{-6} A for VD = 5 V, and the off current (Ioff) is low at 1.59×10^{-11} A, μsat of 0.06 cm^2/V-s and a threshold voltage (Vth) of 15.6 V. Fig. 4(b) displays drain current-drain voltage (ID-VD) output characteristic curves of the ZnO channel annealed at 300 °C; the figure shows an n-type TFT behavior operating in the enhancement mode. This study demonstrates flexible ZnO TFT operation for a device fabricated at a low temperature of 300 °C, as well as on polyimide substrates.

(a)



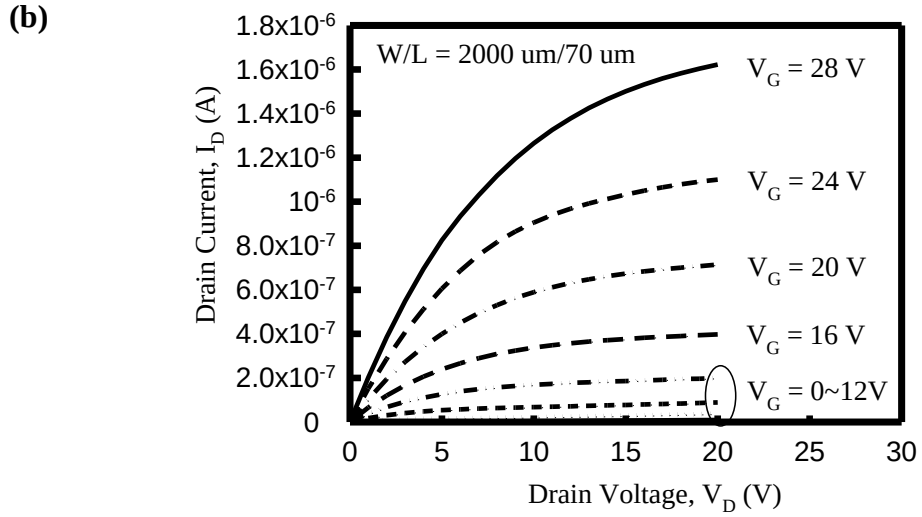
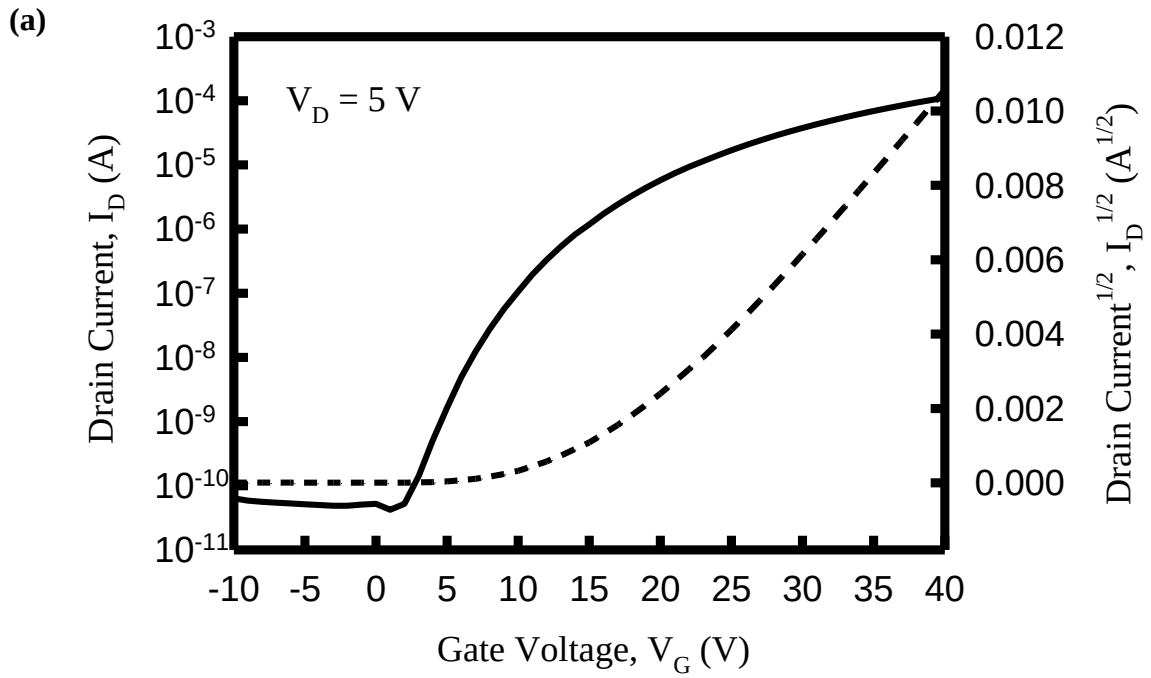


Figure 4. (a)Transfer characteristics curves of ZnO TFT annealed at 300℃ by sol-gel method, VD = 5 V. (b) Output characteristics curves of ZnO TFT annealed at 300℃ by sol-gel method, VG = 0 to 28 V (step 4 V).

Fig. 5(a) shows the transfer characteristics curves of a flexible ZnO TFT with a channel length of 70 μm and a channel width of 2000 μm on polyimide, which has a high on current (Ion) of 1.15 × 10^{-4} A and an off current (Ioff) of 9.25 × 10^{-11} for VD = 5 V. The flexible ZnO TFT exhibited an on-off current ratio (Ion/off) of up to nearly 10^7. The threshold voltage (Vth) was 12.3 V, and the μsat was 0.98 cm^2/V-s. Fig. 5(b) shows the drain current-drain voltage (ID-VD) output characteristics curves of the ZnO channel annealed at 300 °C, demonstrating an n-type flexible ZnO TFT behavior operating in the enhancement mode.



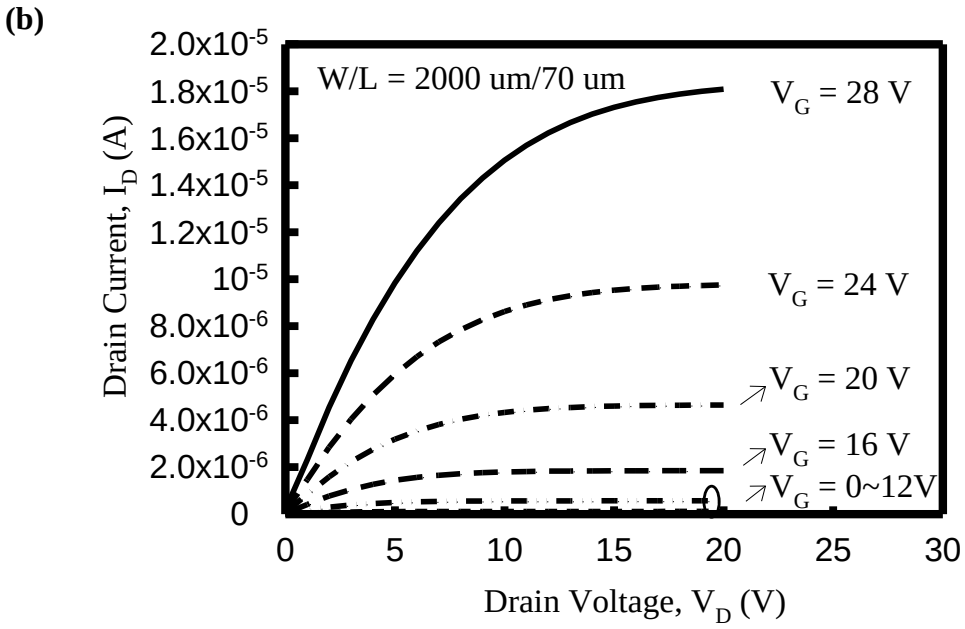


Figure 5. (a)Transfer characteristics curves of flexible ZnO TFT annealed at 300℃ by sol-gel method, VD = 5 V. (b) Output characteristics curves of flexible ZnO TFT annealed at 300℃ by sol-gel method, VG = 0 to 28 V (step 4 V).

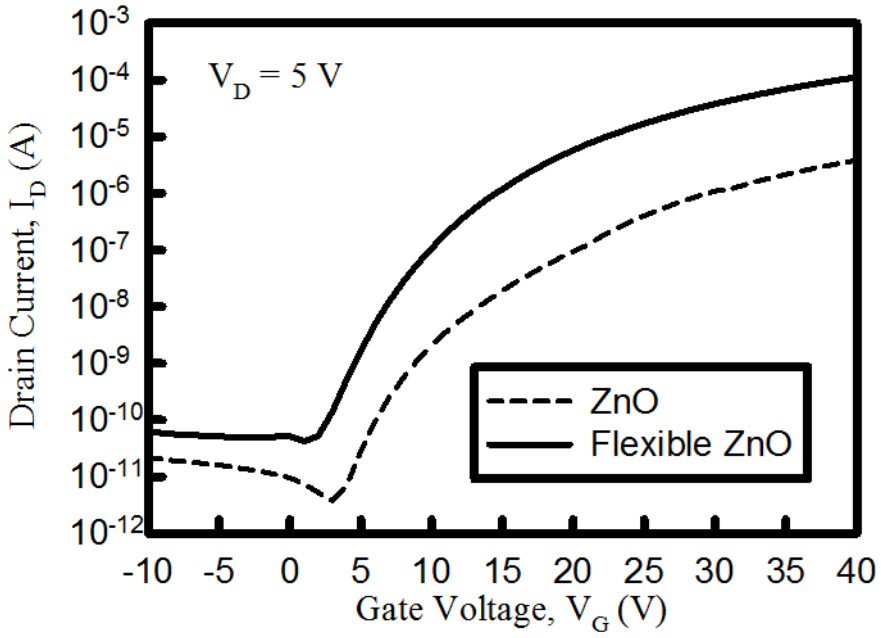


Figure 6. Transfer characteristics curves of both flexible ZnO TFT and ZnO TFT annealed at 300℃ by sol-gel method, VD = 5 V.

Fig. 6 shows the transfer characteristics for ZnO on the different polyimide substrates and silicon. The flexible ZnO TFT mobility increases dramatically because of introduced stress; therefore,

the TFT's on-currents on the polyimide substrates were better compared with the transistor manufactured on the silicon substrates [13].

4. CONCLUSIONS

This study demonstrates a simple method of fabricating ZnO TFT and flexible ZnO TFT by the sol-gel method and annealing at low temperatures (300 °C). The sol-gel method growth of the semiconductor layer does not require a vacuum system. Experimental results indicate that ZnO TFT and flexible ZnO TFT are better or at least comparable to a conventional transistor, and the flexible ZnO TFT exhibits superior electrical performance. The flexible ZnO TFT exhibited an on-off current ratio (Ion/off) up to nearly 10^7, and the μsat was 0.98 cm^2/V-s.

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