

## A Semi-experimental Method for Fast Evaluation of the Performance of Grid-type Dye-sensitized Solar Module

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Received: 30 April 2013 / Accepted: 8 June 2013 / Published: 1 July 2013

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A semi-experimental method is developed to evaluate the performance behavior of grid-type dye-sensitized solar module based on information from a small cell. By assuming uniform photo-current distribution and cell properties being independent of substrate size, IV curves of various modules can be predicted. In comparison, the fill factor (FF) actually measured agrees well to the calculated number although short-circuit current density ( $j_{SC}$ ) is somehow lower than the predicted value, probably due to inconsistency during module fabrication. This method provides a fast and simple way to evaluate new materials and processes for large area platform without the need for detailed knowledge of each component for a full theoretical model.

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**Keywords:** dye-sensitized; grid-type; fill factor

### 1. INTRODUCTION

Dye-sensitized Solar Cell (DSSC) has caught much attention for its potential to furnish low cost solar electricity due to its inherent features such as abundant raw materials, simple manufacturing process and low energy payback time [1-3]. To date, over 10% energy conversion efficiency cell has been developed by incorporating Ruthenium complex sensitizers, highly-volatile electrolyte and thermal-deposited platinum counter electrode on conductive glass substrate with active area less than 1 cm<sup>2</sup> [4]. More recently, various module structures with active areas ranging from several square centimeters to hundreds of square centimeters were tested to explore its feasibility for practical use [5-11]. However the test cost is understandably high due to its size.

In a convention way to predict the behavior of large DSSC, mathematical modeling was developed by firstly simulating the current-voltage behavior (IV curve) of small cell from an ideal diode equation and then using this model to predict the IV curve of large module by taking into consideration the resistive losses and interfacial recombination [12-16]. In particular, how to deal with multiple interfaces including transparent conductive oxide (TCO)/TiO<sub>2</sub> film, Dye/TiO<sub>2</sub> film, TiO<sub>2</sub> film/electrolyte and electrolyte/catalyst in the modeling equations remains uncertain, which usually leads to lengthy and complex equations. Moreover, the properties of those interfaces are strongly dependent on the fabrication techniques as well as properties of raw materials inside the devices, so the effectiveness of each model remains questionable for general use. Consequently, to develop a simple and common method to predict module performance is necessary for researchers for fast evaluation of module performance.

In this study, we proposed a semi-experimental method to predict the IV curve, especially the fill factor (FF) of grid-type DSSC module based on information from a small cell. This small cell is designed to have identical raw materials and interface properties to the module except substrate size. So the complicated interfaces and possible variations of raw materials between cell and module can be efficiently offset by experimental skills without the need for detailed analysis of each individual resistance, only resistive loss relating to size is considered. In order to prove the usefulness of our model, we prepared small cell and large module with the same raw materials and by the same process. So if the simulated result based on small cell data matches well the measured data of large module, our goal of developing a simplified model is achieved.

## 2. EXPERIMENTAL

The detail of fabricating cell and grid-type module has been published elsewhere [17]. Briefly, bi-layer TiO<sub>2</sub> films (with total thickness of around 14μm) with designed TiO<sub>2</sub>/Ag grid pattern are coated on FTO glass (NSG, 3.1mm, 9 Ω/sq) by screen printing active TiO<sub>2</sub> paste (PNT series, Tripod, Taiwan, average particle size=18-20nm), scattering TiO<sub>2</sub> paste (JGC&C PST400C, Japan) and silver paste (EPI Technology, Taiwan, PTG series). After the coating process is completed, the substrate is sintered at 325°C for 30 minutes, 375°C for 30 minutes, 450°C for 30 minutes and 500°C for 30 minutes sequentially in a programmable oven with atmosphere control. After sintering process, the hot-melt film (Surlyn 1706, 30μm) with pre-punched pattern that fits cell or module's shape is covered on printed TiO<sub>2</sub> film and then sent into a programmable hydraulic hot-presser at 100°C for 3 minute in a vacuum chamber. The purpose of this treatment is to protect Ag line from possible damage in later processes like dye soaking and electrolyte injection as well. Finally, dye impregnation is done by immersing the afore-prepared TiO<sub>2</sub> electrode in a 0.4 mM N719 ethanol solution at 40°C for 5 hours in a programmable dyeing tank to finish photo-anode preparation.

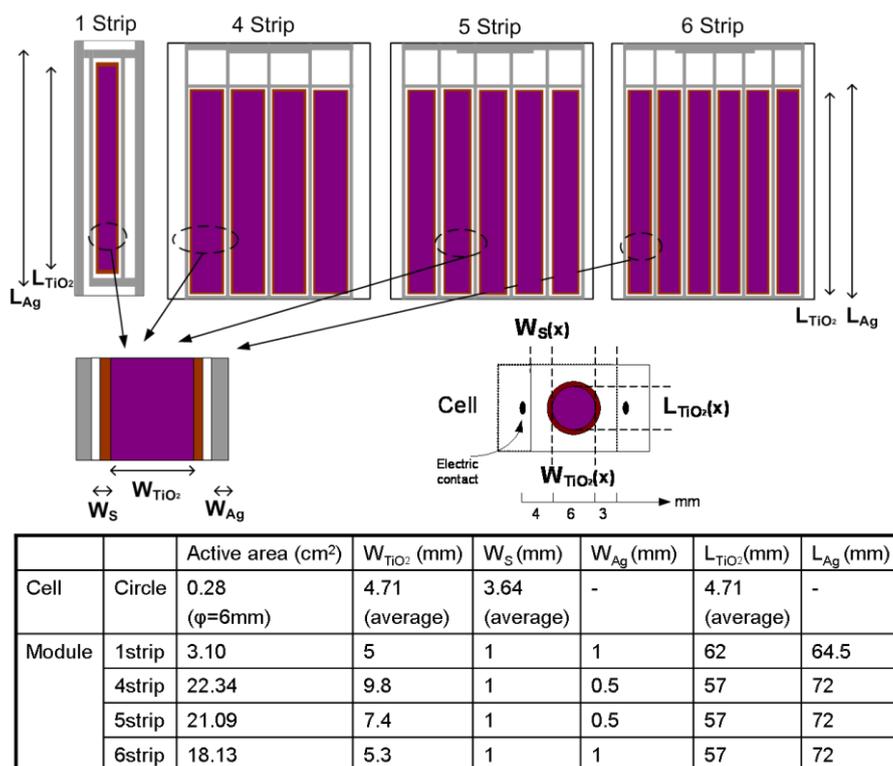
For making the counter electrode, injection holes are pre-drilled before making counter electrode to facilitate the following electrolyte injection process. A novel nano-Pt counter electrode [18-21] is used to fabricate counter electrodes in this study: Ag grid is first screen-printed and sintered at 500°C for 30minutes on FTO glass (NSG, 3.1mm, 9Ω/sq) for modules; then the aforementioned pre-

punched hot-melt film is attached and hot-pressed on the substrate to protect Ag pattern or a small piece of bare FTO glass (for cell). When the Ag pattern is well protected, it is rinsed in an aqueous bath containing commercial TCO cleaner (2% of PK-LCG545) and then immersed into a solution containing 4% conditioner (ML371, Rockwood) at 60°C for 5 minutes, the purpose of this treatment is to change the surface charge state of FTO surface to facilitate nano-particle adsorption. Then the conditioned substrate is immersed into nano-Pt solution to adsorb a very thin layer of nano-Pt to finish electrode preparation.

The as-prepared dye-sensitized electrode and counter electrode are laminated by placing them face to face in a hydraulic hot-presser at 110°C in a vacuum chamber for 4 minutes until the boundary of the two hot-melt films disappears. The device is then removed out from the hot-presser and cooled down in a second presser to ambient temperature. Electrolyte solution containing 0.2M DMPII, 0.2M LiI, 0.2M TBAI, 0.05M I<sub>2</sub> and 0.5M 4-tert butyl pyridine (TBP) in 3-methoxypropionitrile (MPN), is injected into the gap formed by the hot-melt films via the pre-drilled hole on the counter electrode side by a pumping injector. Finally, the injection holes are hot sealed by a piece of thin cover glass with a hot-melt film underneath as adhesive.

The IV curve of cell and module are both measured in 4-terminal jack to minimize the possible contact resistance with a computer-controlled digital source meter (Keithley 2400) under AM1.5, 1 Sun illumination (YAMASHITA DENSO YSS-150A).

### 3. DISCUSSION



**Figure 1.** Dimensional parameters of cell and module in this study. Note that W<sub>TiO<sub>2</sub></sub>, W<sub>S</sub> and L<sub>TiO<sub>2</sub></sub> of cell are averaged.

The series resistance,  $R_s$ , of a DSSC is related to many sub-resistances as shown below:

$$R_s = f(R_{contact}, R_{TCO}, R_{Ag}, R_{electrolyte}, R_{Pt})$$

In which  $R_{contact}$  is the contact resistance between terminals and measuring clip,  $R_{TCO}$  is the sheet resistance of TCO glass,  $R_{Ag}$  is the silver grid resistance,  $R_{electrolyte}$  is the ohmic drop across electrolyte layer and  $R_{Pt}$  is the overpotential loss on Pt counter electrode. Generally, we need to deal with each of them in the module structure and then calculate the IV curve; but now since the cell and modules are prepared identically, we can reasonably assume  $R_{contact}$ ,  $R_{electrolyte}$  and  $R_{Pt}$  and interfacial properties are the same in cell and modules, and the only difference between them is the  $R_{TCO}$  and  $R_{Ag}$  because of different substrate size and geometry. This treatment not only simplifies the prediction process but also is effective for a device made with different raw materials and fabrication processes.

Figure 1 summarizes the dimensional parameters of small cell and modules in this study and Figure 2 shows the experimental IV curve of the cell (solid line) with short circuit current density ( $j_{sc}$ ), open circuit voltage ( $V_{OC}$ ) and fill factor (FF) to be 14.94 mA/cm<sup>2</sup>, 0.72V and 0.63 respectively, leading to a 6.77% conversion efficiency; which is typical for DSSC of 0.28cm<sup>2</sup> in size and employing with N719 sensitizers and MPN-based electrolyte without pre- and post-treatment on TiO<sub>2</sub> films [22]. Now we consider the voltage drop ( $\Delta V$ ) due to resistive loss inside this small cell as follows:

$$\Delta V = I \times \rho_{TCO} \times \left( \frac{W_{TiO_2} + 2W_s}{L_{TiO_2}} \right) \tag{1}$$

Equation (1) describes the uncompensated voltage loss when current passes TCO glass before it is measured for the cell fabricated with TCO glass with identical sheet resistance, where  $I$  is current of the cell,  $\rho_{TCO}$  is sheet resistance of FTO glass (9Ω/sq in this study),  $W_{TiO_2}$  is the width of TiO<sub>2</sub> film,  $W_s$  is the width of seal structure and  $L_{TiO_2}$  is the length of the cell.

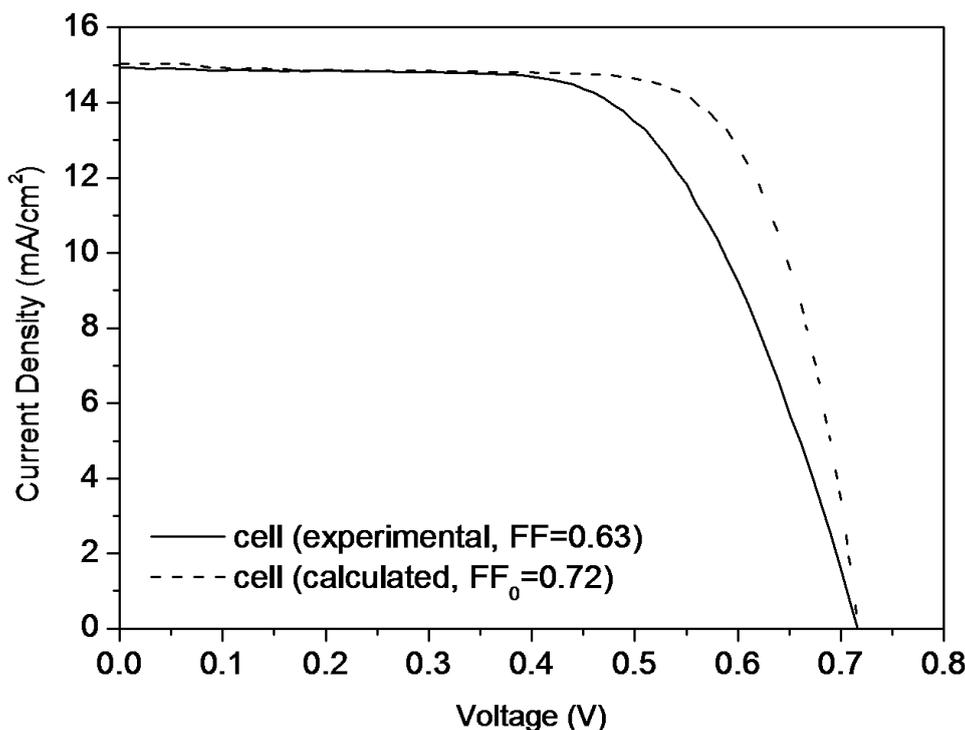


Figure 2. Measured (solid line) and calculated (dotted line) IV curve of 0.28cm<sup>2</sup> cell.

Assuming the current is homogeneously generated on the film, then

$$I = j \times A \tag{2}$$

Where  $j$  is the measured current density ( $\text{mA}/\text{cm}^2$ ) and  $A$  is the active area of the electrode. Combining equations (1) and (2), the voltage drop due to series resistance in IV curve is:

$$\Delta V = j \times \rho_{\text{TCO}} \times [(W_{\text{TiO}_2})^2 + 2W_{\text{TiO}_2}W_s] \tag{3}$$

By defining  $R_{\text{TCO}} = \rho_{\text{TCO}} \times [(W_{\text{TiO}_2})^2 + 2W_{\text{TiO}_2}W_s]$ , we can deduct  $\Delta V$  of the small cell and re-plot IV curve on Figure 2 (dotted line). It is found that FF of the new IV curve,  $\text{FF}_0$ , becomes 0.72, this value can be regarded as representing a cell having the same interface behavior and materials but without the influence of  $R_{\text{TCO}}$ .

Further analyzing equation (3) shows that dramatic voltage drop on IV curve will happen if one directly increases active area without placing current collector near active area because of large  $W_{\text{TiO}_2}$  and  $W_s$ . Therefore, in the module platform, silver paste was screen-printed to form grid lines along  $\text{TiO}_2$  strip. The resistance of silver lines is calculated by:

$$R_{\text{Ag}} = \rho_{\text{Ag}} \frac{L_{\text{Ag}}}{h_{\text{Ag}} W_{\text{Ag}}} \tag{4}$$

Where  $\rho_{\text{Ag}}$  is the resistivity of silver line,  $L_{\text{Ag}}$ ,  $h_{\text{Ag}}$  and  $W_{\text{Ag}}$  are the length, thickness and width of silver line, respectively. In this study,  $\rho_{\text{Ag}} = 9 \times 10^{-8} \Omega\text{cm}$  and  $h_{\text{Ag}} = 7 \mu\text{m}$ . By calculating  $R_{\text{TCO}}$  and  $R_{\text{Ag}}$  for different modules, the voltage drop of modules can be derived as follows:

$$\Delta V = j \times [R_{\text{TCO}} + R_{\text{Ag}}] \tag{5}$$

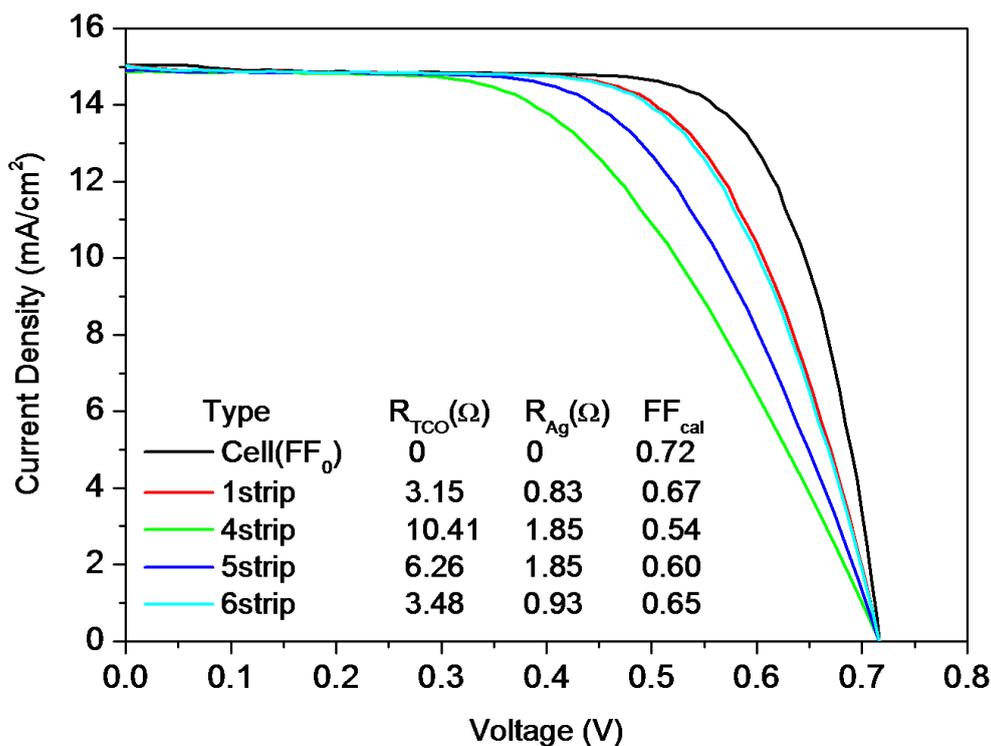
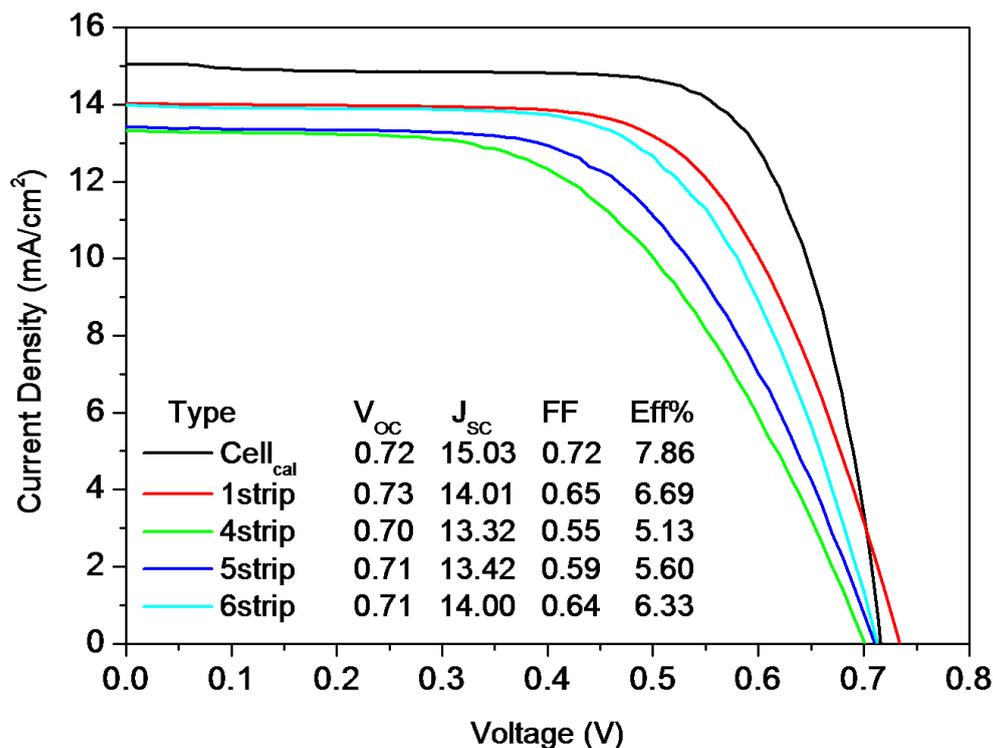


Figure 3. Calculated  $R_{\text{TCO}}$  and  $R_{\text{Ag}}$  and estimated IV curves of 1strip, 4strip, 5strip and 6strip modules.



**Figure 4.** Measured IV curves of 1strip, 4strip, 5strip and 6 strip modules; IV parameters are also listed.

Figure 3 illustrates the calculated  $R_{TCO}$  and  $R_{Ag}$  as well as estimated IV curves for modules derived from  $R_{TCO}$ -free IV curve (dotted line in figure2). First of all, it is apparent that  $R_{TCO}$  influences  $\Delta V$  more than  $R_{Ag}$  does. In addition, we can find that small  $W_{TiO_2}$  and  $W_S$  are essential for good resistive control but in reality, small  $W_{TiO_2}$  results in low total power output and small  $W_S$  challenges sealing skill. Therefore, there exists an optimization of dimensional parameters in module design.

As shown in Figure 4, real grid-type modules were fabricated and measured. And its comparison with predicted data can be made by a comparison between Figure 3 and Figure 4. First, the calculated IV curves agrees well to real ones especially FFs, indicating this simple method can effectively offset interfacial effects in DSSC and consequently we can concentrate on the influence of geometric-related resistive loss only during the scaling up work. Secondly, according to previous studies [11, 23], the  $j_{sc}$  of modules should be equal to that of small cell before dramatic FF loss happens; In our experiments, even the worst-performed 4-strip-type can still maintain a FF of 0.55, meaning the control of series resistance is adequate; however, smaller  $j_{sc}$  was observed in real module IV curves than the cell value. This result suggests that either photo-current is not homogenously generated or the fabricating process is not stable enough in all experiments. Notwithstanding these drawbacks, this method avoids dealing with puzzling interfacial issues and provides a fast and reliable way to predict IV behaviors of large modules.

### 3. CONCLUSIONS

In conclusion, a semi-experimental method has been developed to predict the performance of grid-type DSSC module from the IV behavior of small cell. With proper experiment designs and skills, it is possible to predict module behavior by only focusing on resistive loss relating to the module size. Future optimization of this method can be realized by stabilizing device fabrication technique as well as electrode uniformity to further improve its accuracy.

### ACKNOWLEDGEMENTS

The authors are very grateful to the National Science Council in Taiwan for its financial support under contract no. NSC-101-2218-E-007-010

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